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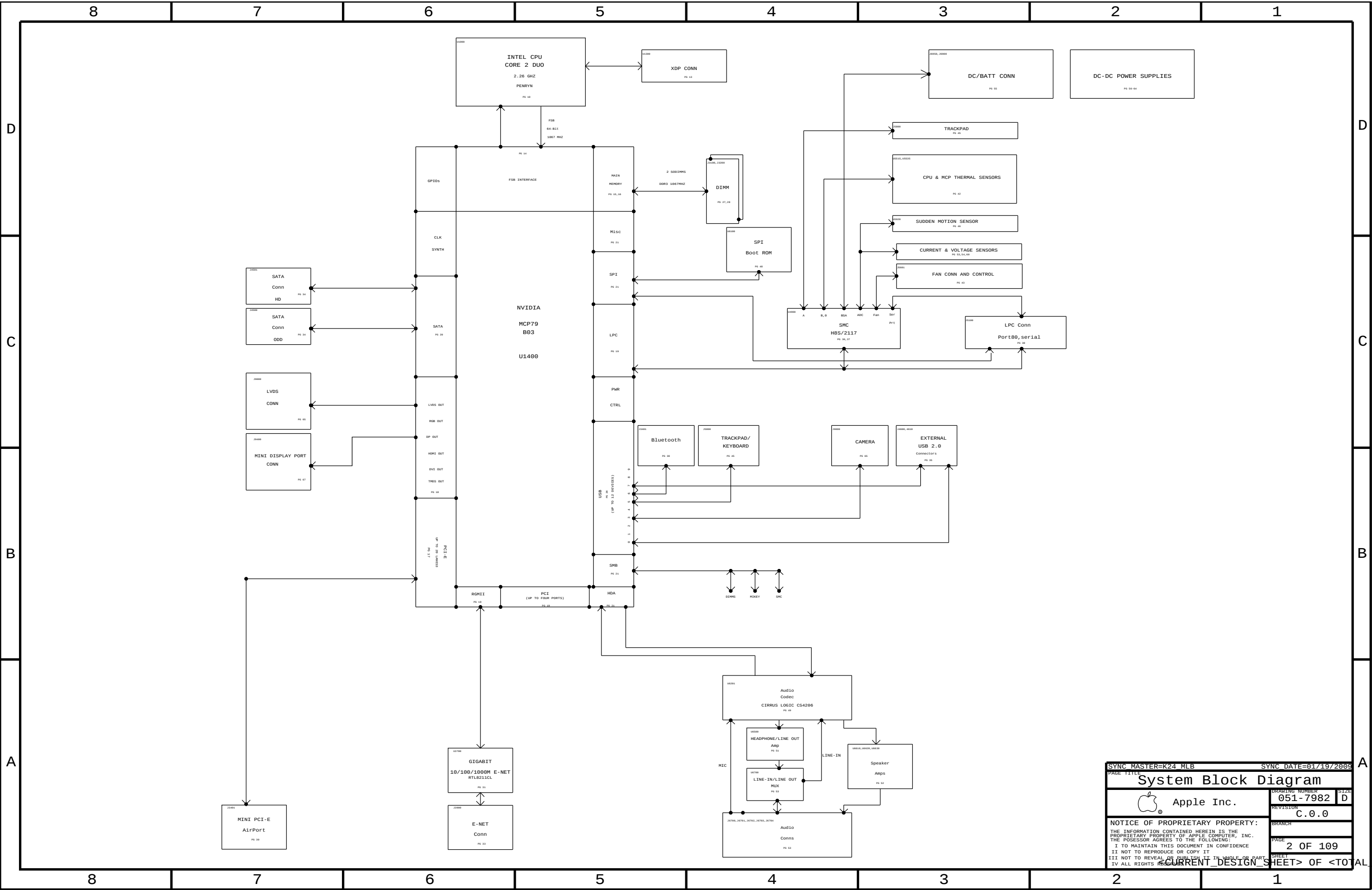
SCHEMATIC, "Okashi"

11/01/2009

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SYNC MASTER=K24 MLB

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System Block Diagram

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K84 POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture for the K84 platform, showing the flow of power from the AC adapter and battery through various regulators and controllers to the CPU and other system components.

Key Components and Connections:

- AC Adapter and Battery:** The AC adapter (J6950) provides DCIN (16.5V) to the PBUS SUPPLY/BATTERY CHARGER (ISL6258AHRZ, U7000). The battery (BATT_POS_F) is connected to the charger via a 6A fuse (F6905).
- Power Distribution:** The charger outputs power to the PBUS (PPBAT_G3H_CHGR_REG) and the CPUVTT (TPS5117, U7600) regulator. The CPUVTT regulator provides power to the CPU (U1000) via the CPUVTT_S0_REG.
- Regulators and Controllers:**
 - TPS51125 (U7200):** A 3.3V regulator providing power to the P3V3S5 and P3V3S3_FET.
 - TPS51116 (U7300):** A 1.5V regulator providing power to the P1V5S0 and P1V5S3_FET.
 - TPS51117 (U7600):** A 1.95V regulator providing power to the CPUVTT.
 - TPS51125 (U7200):** A 3.3V regulator providing power to the P3V3S5 and P3V3S3_FET.
 - TPS51116 (U7300):** A 1.5V regulator providing power to the P1V5S0 and P1V5S3_FET.
 - TPS51117 (U7600):** A 1.95V regulator providing power to the CPUVTT.
- Controllers and Monitors:**
 - SMC (U4900):** System Management Controller providing various control signals (e.g., SMC_RESET_L, SMC_ONOFF_L).
 - MCP79 (U1400):** Memory Controller providing control signals (e.g., PM_SLP_S4_L, PM_SLP_S3_L).
 - TPS51125 (U7200):** A 3.3V regulator providing power to the P3V3S5 and P3V3S3_FET.
 - TPS51116 (U7300):** A 1.5V regulator providing power to the P1V5S0 and P1V5S3_FET.
 - TPS51117 (U7600):** A 1.95V regulator providing power to the CPUVTT.
- Power FETs and Diodes:** Various MOSFETs (e.g., Q7900, Q7910, Q7930, Q7940) and diodes (e.g., D6905, D6906) are used for power switching and protection.

Section Labels: The diagram is divided into sections A, B, C, and D, indicating different functional blocks or power planes.

Legend: The legend defines the symbols used in the diagram, including power planes, regulators, controllers, and components.

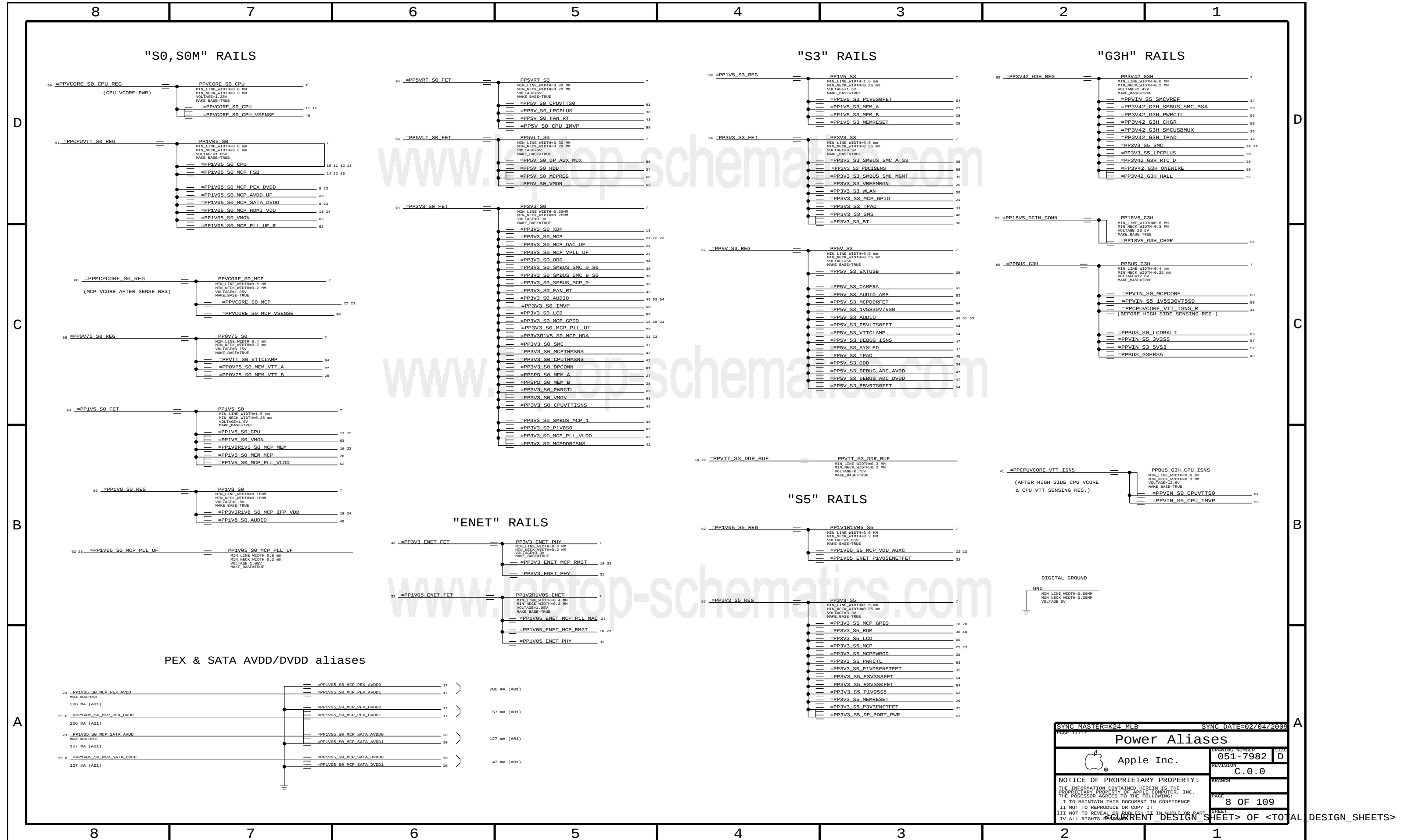
Notes: The notes provide additional information about the components and their connections, including part numbers and functional descriptions.

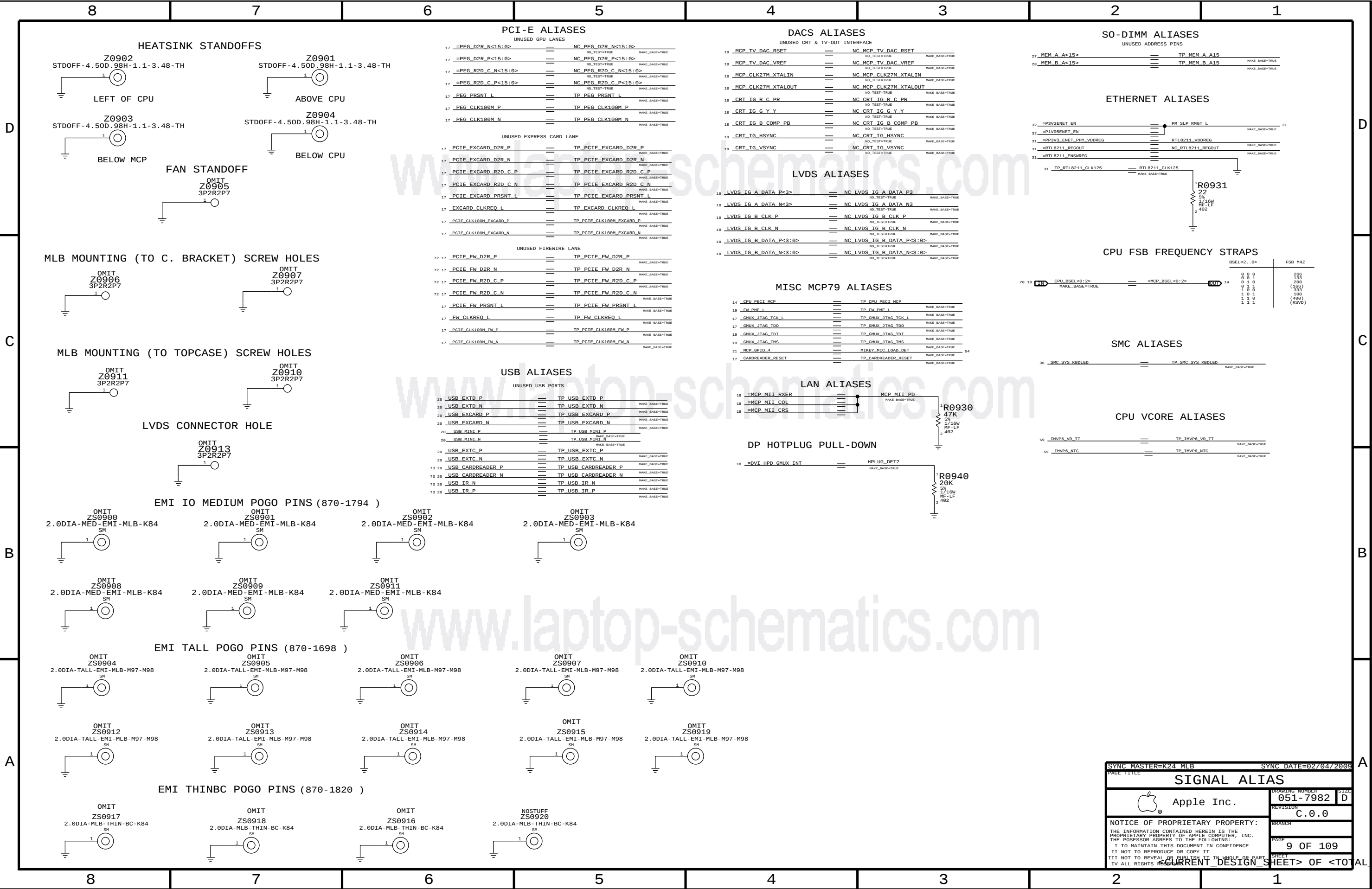
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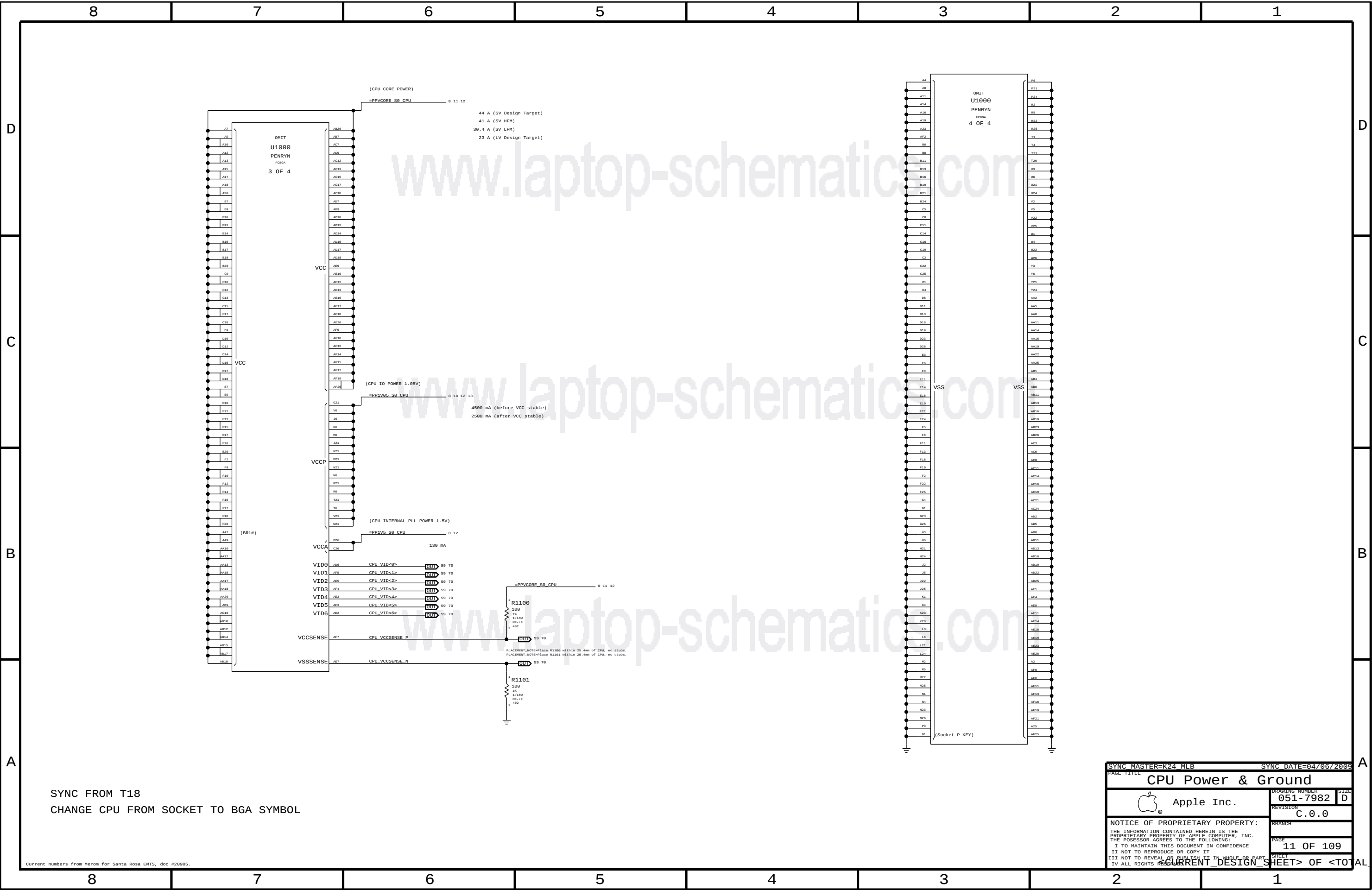
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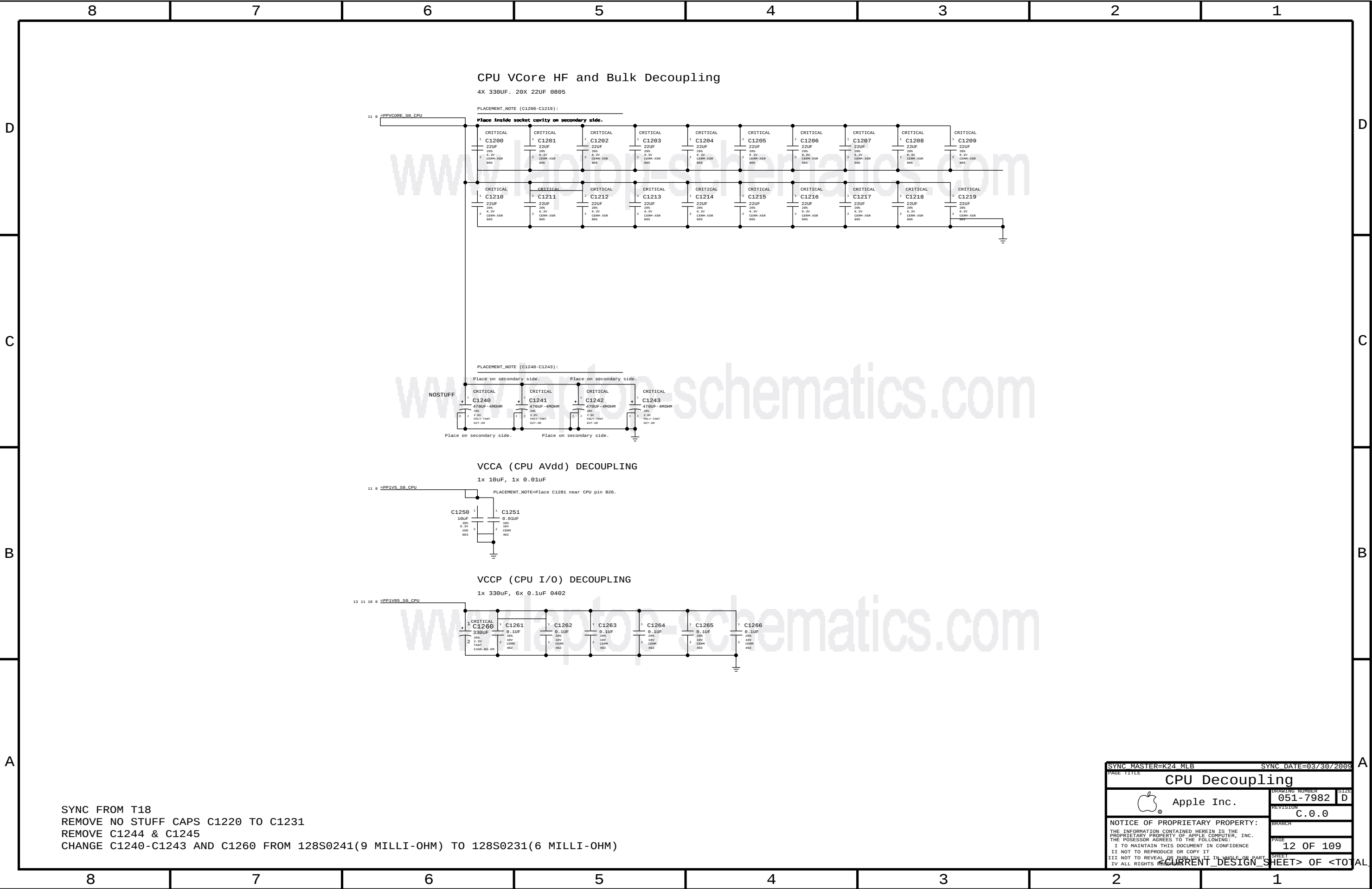






SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

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CPU Power & Ground			
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87654321

SYNC FROM T18

REMOVE NO STUFF CAPS C1220 TO C1231

REMOVE C1244 & C1245

CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

87654321

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CPU Decoupling

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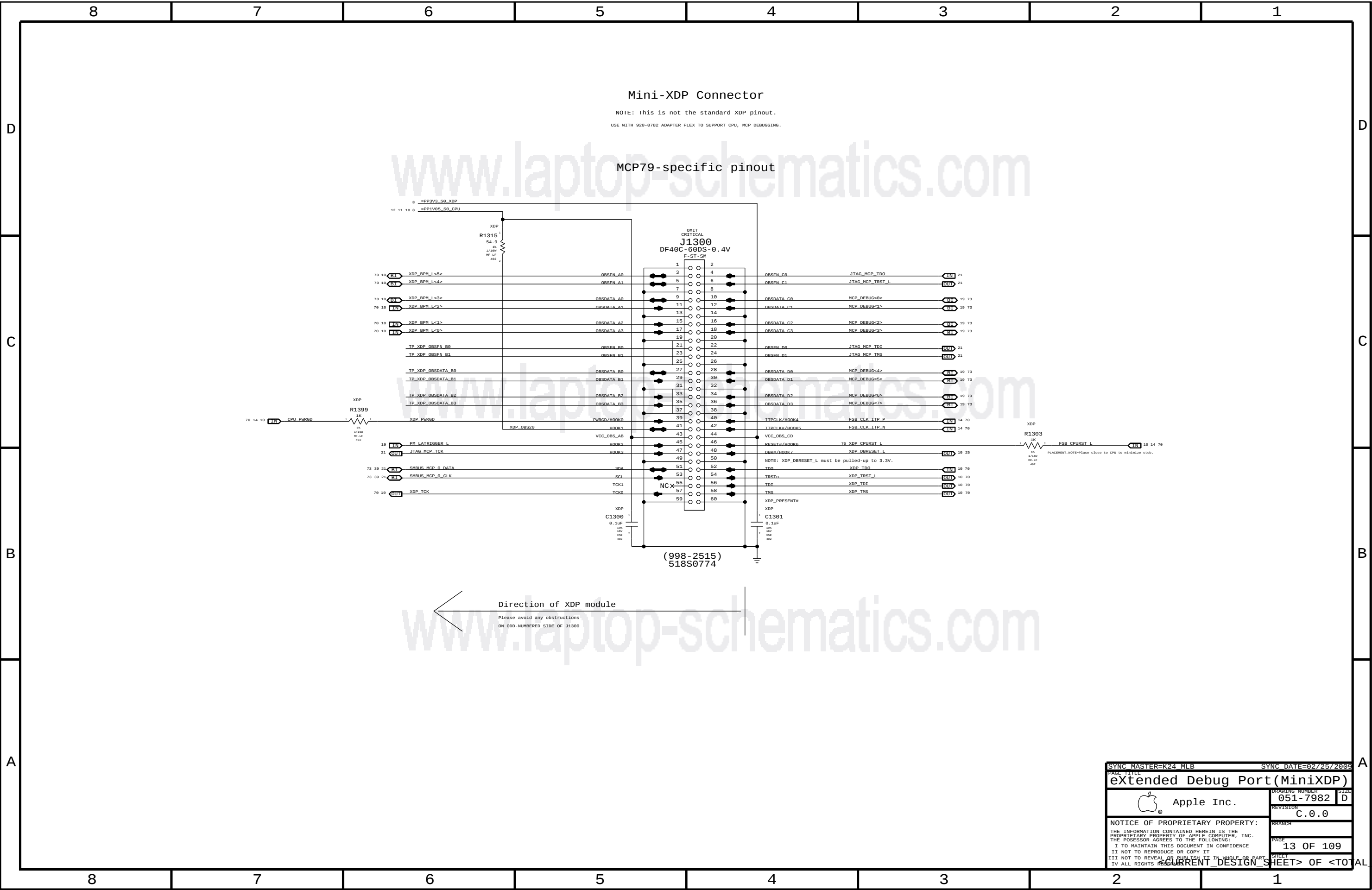
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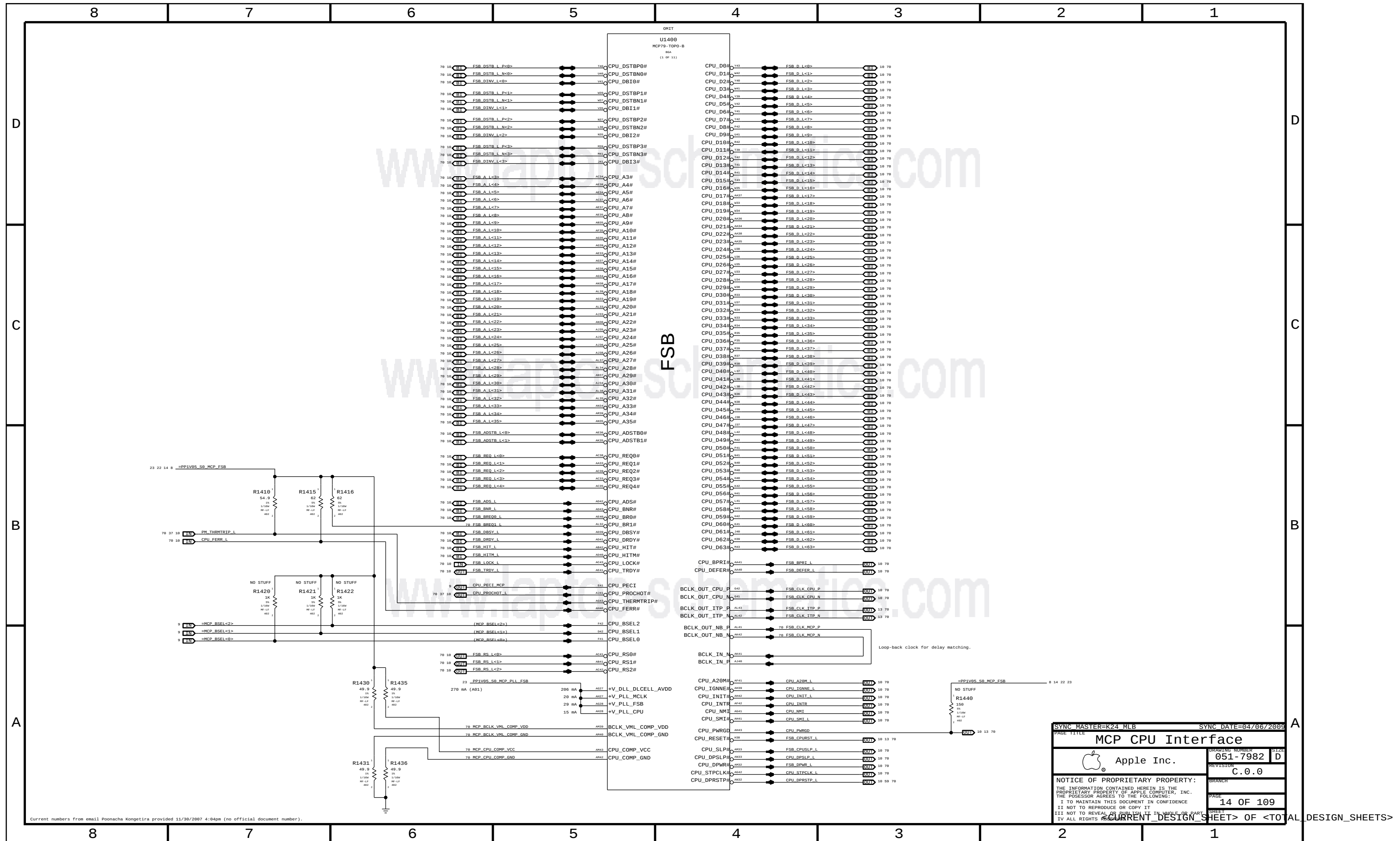
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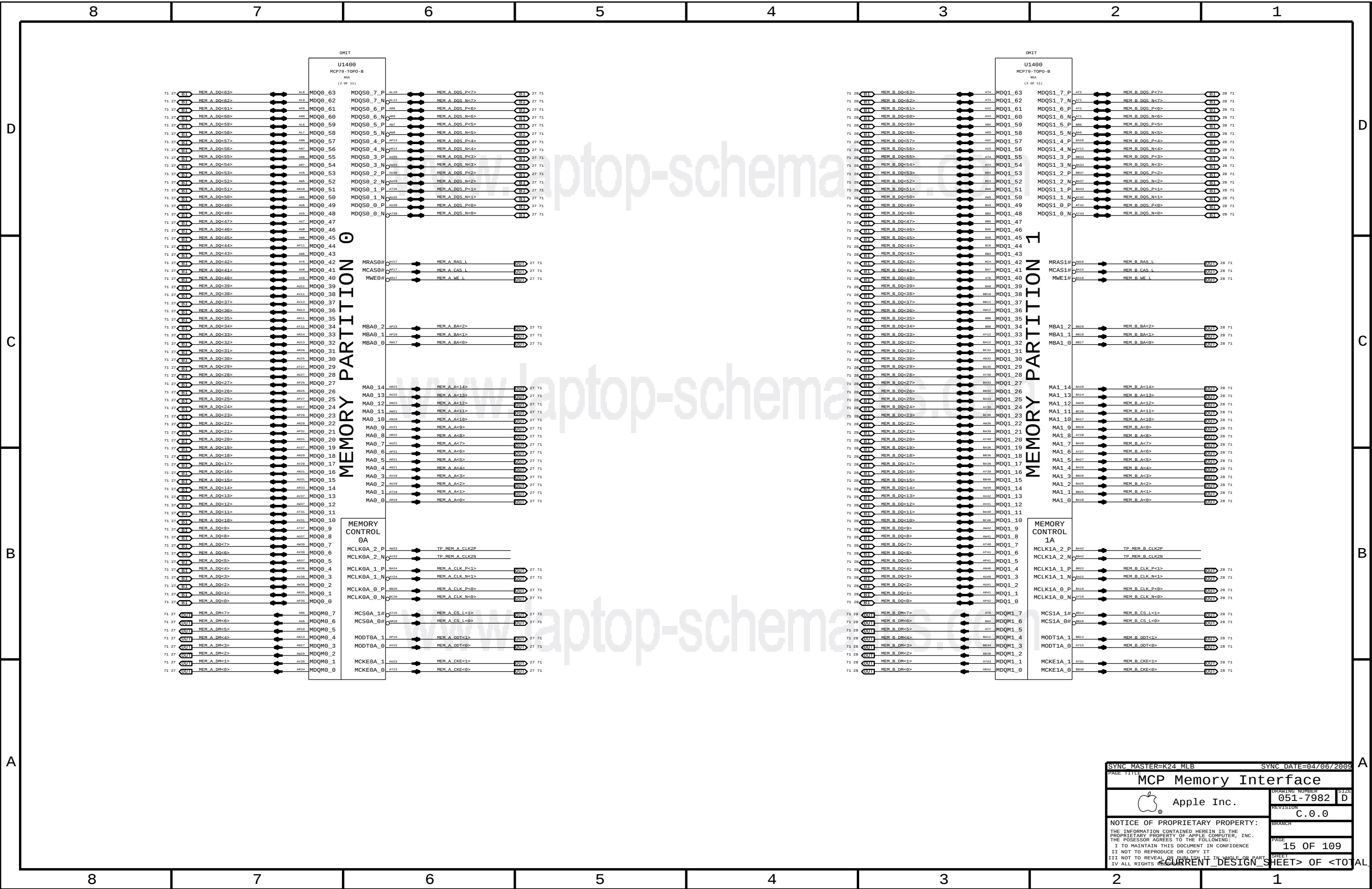
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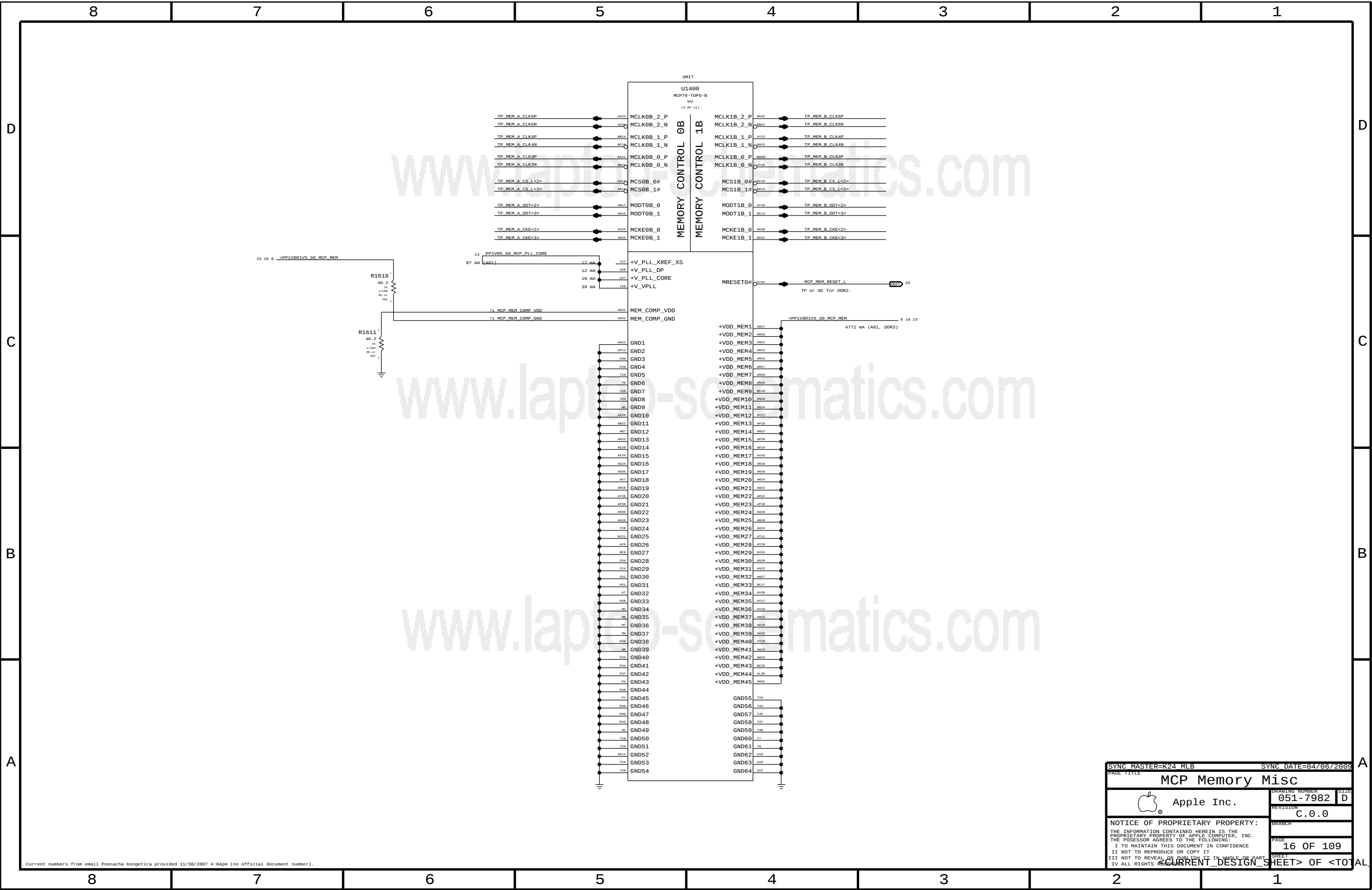
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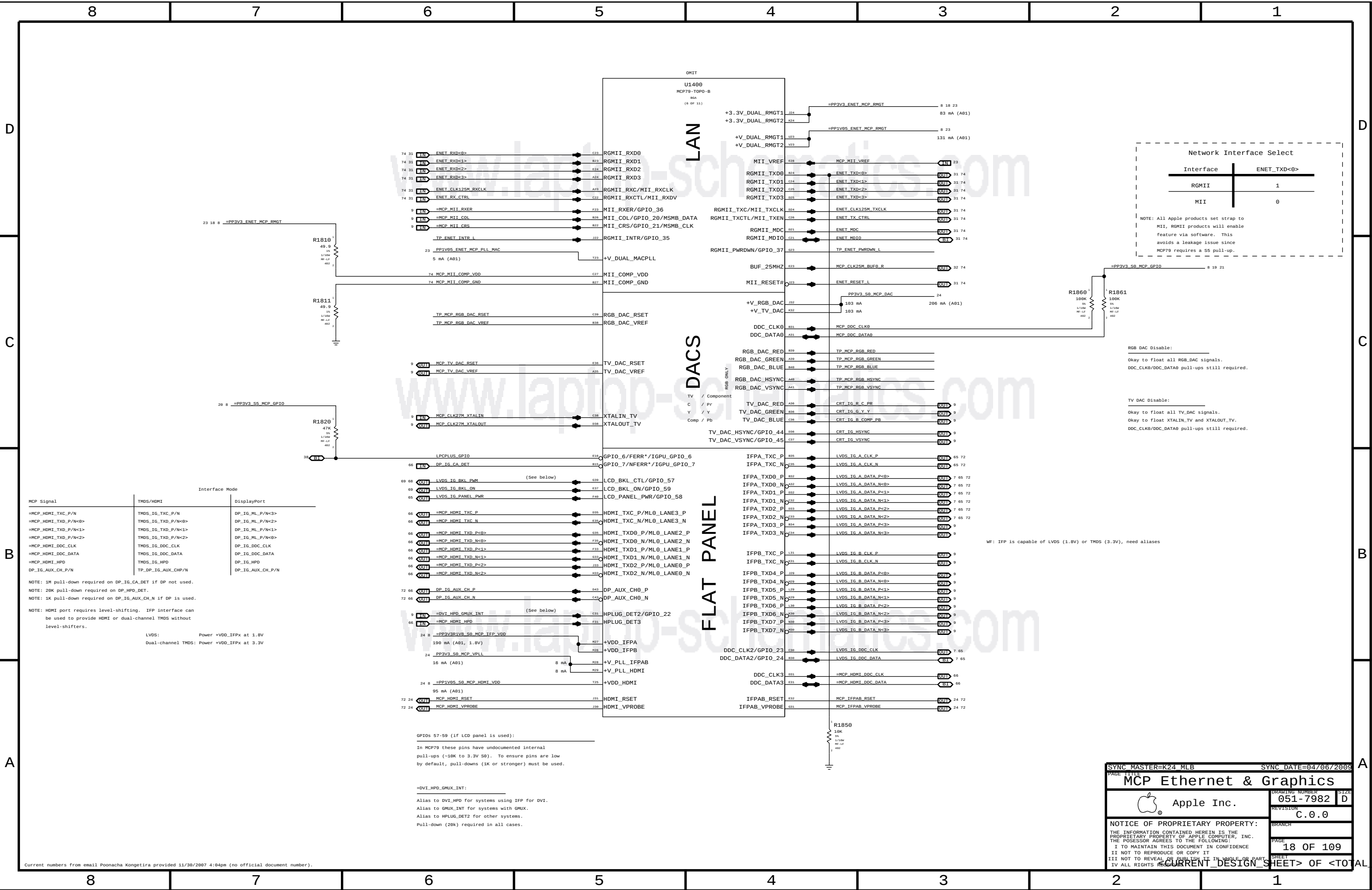
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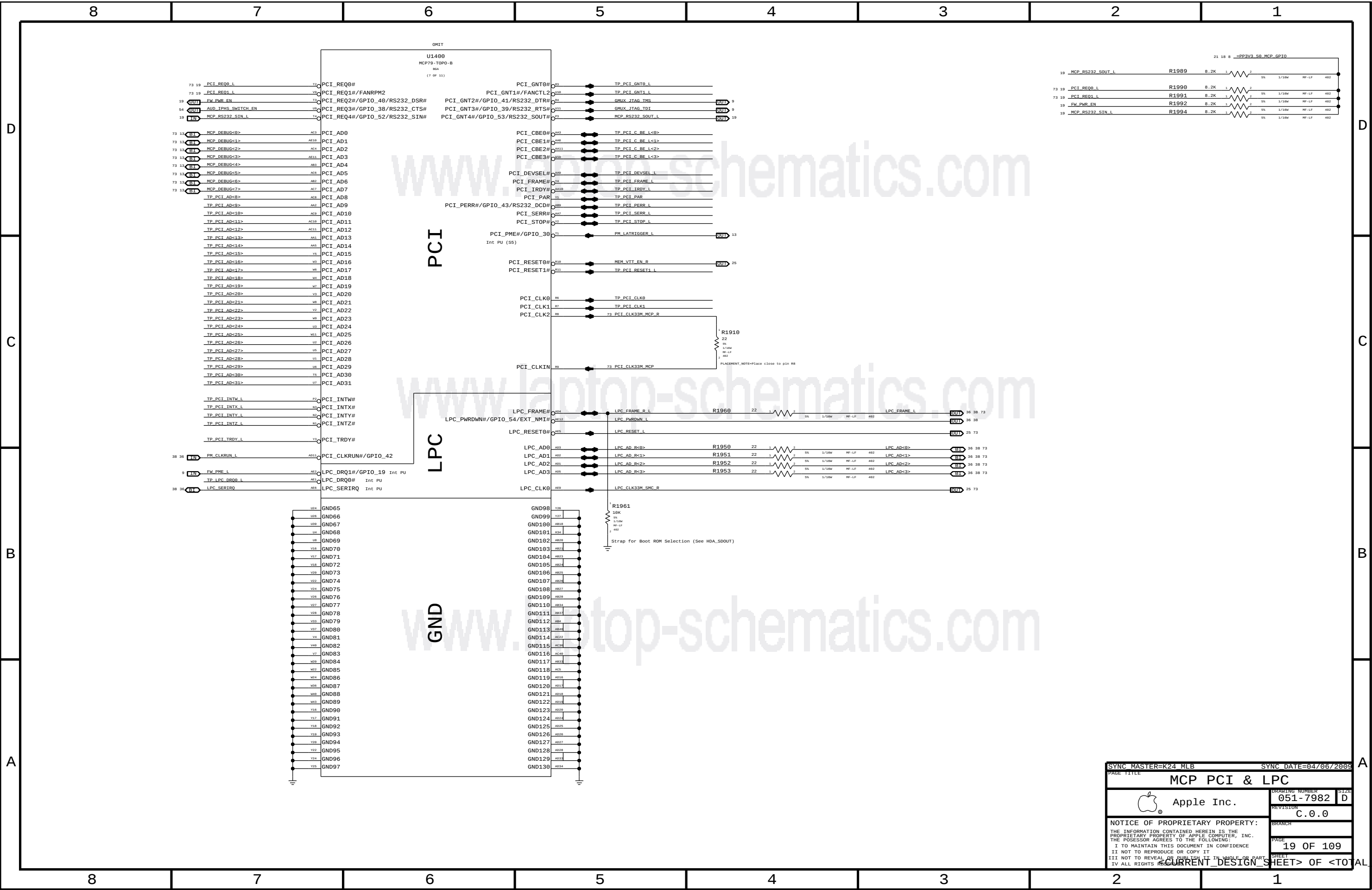


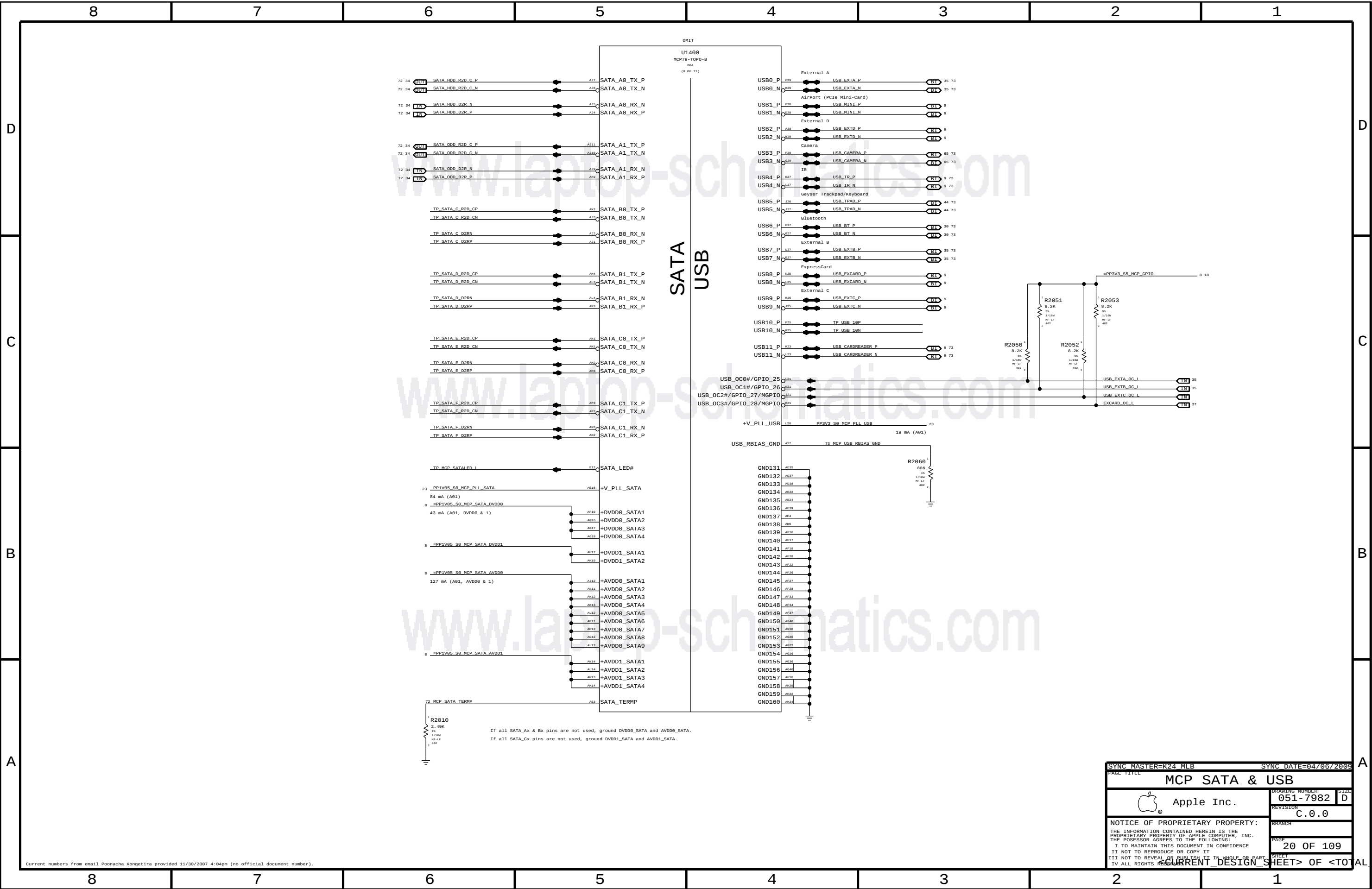




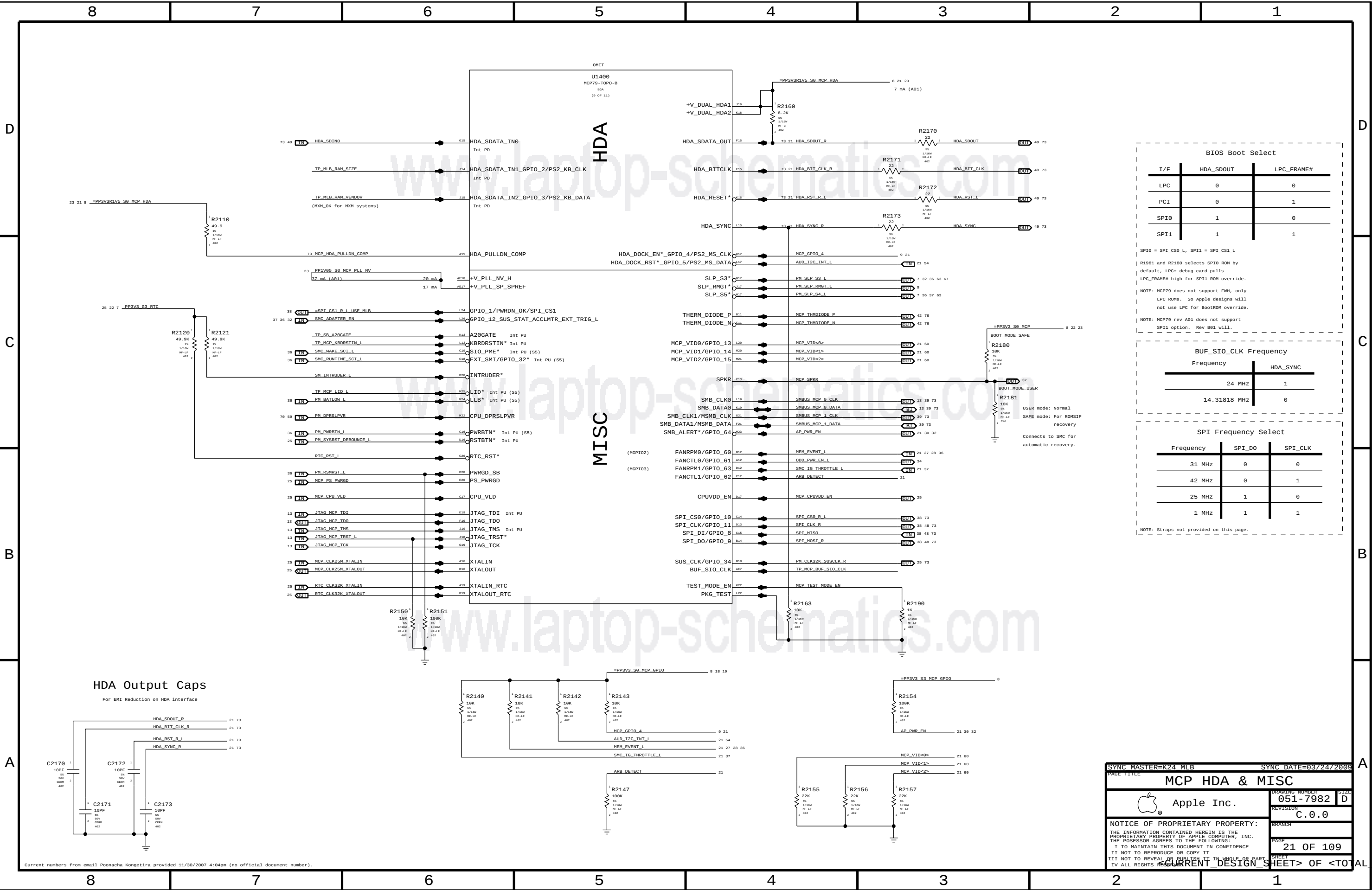








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BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

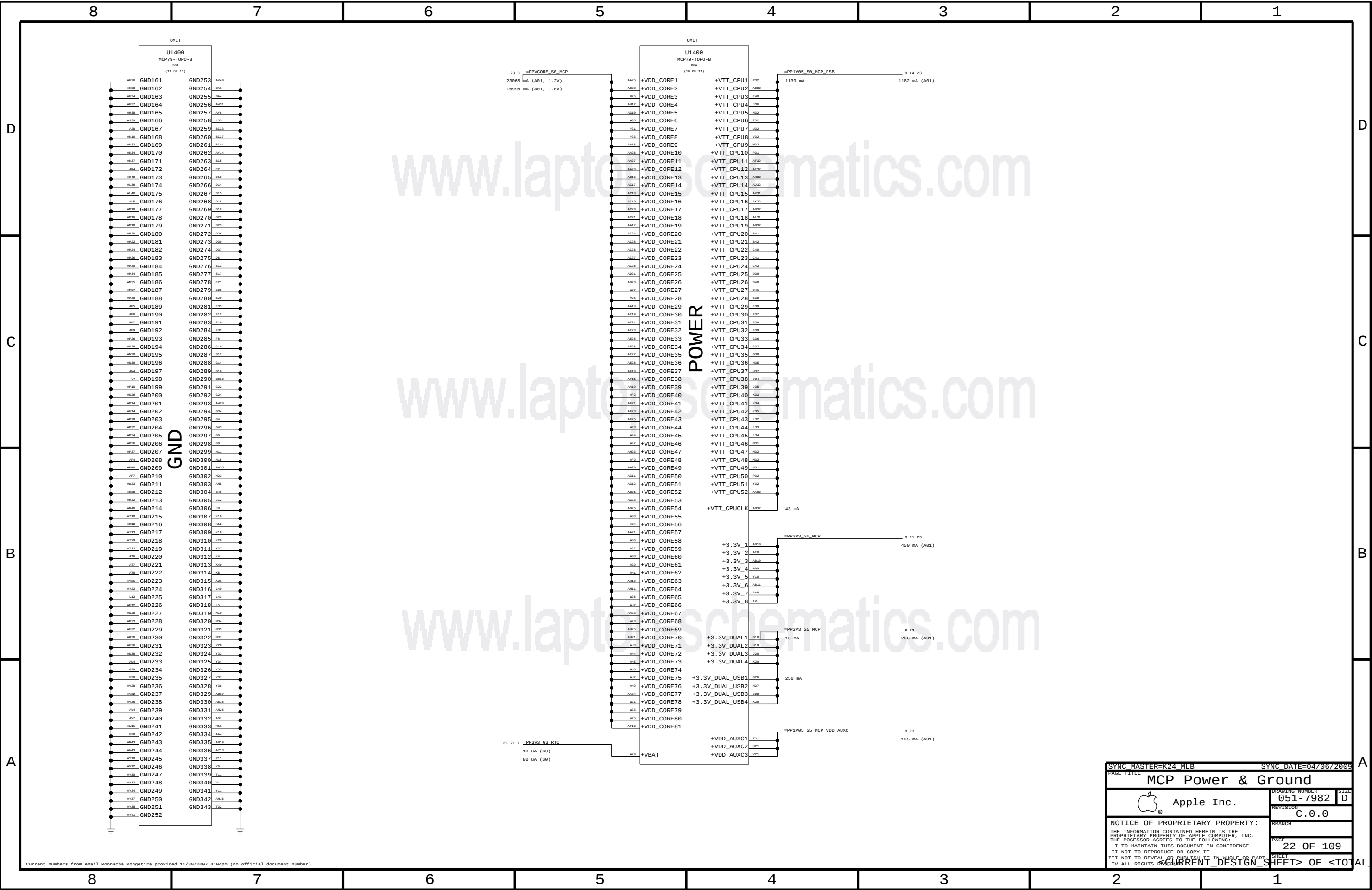
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

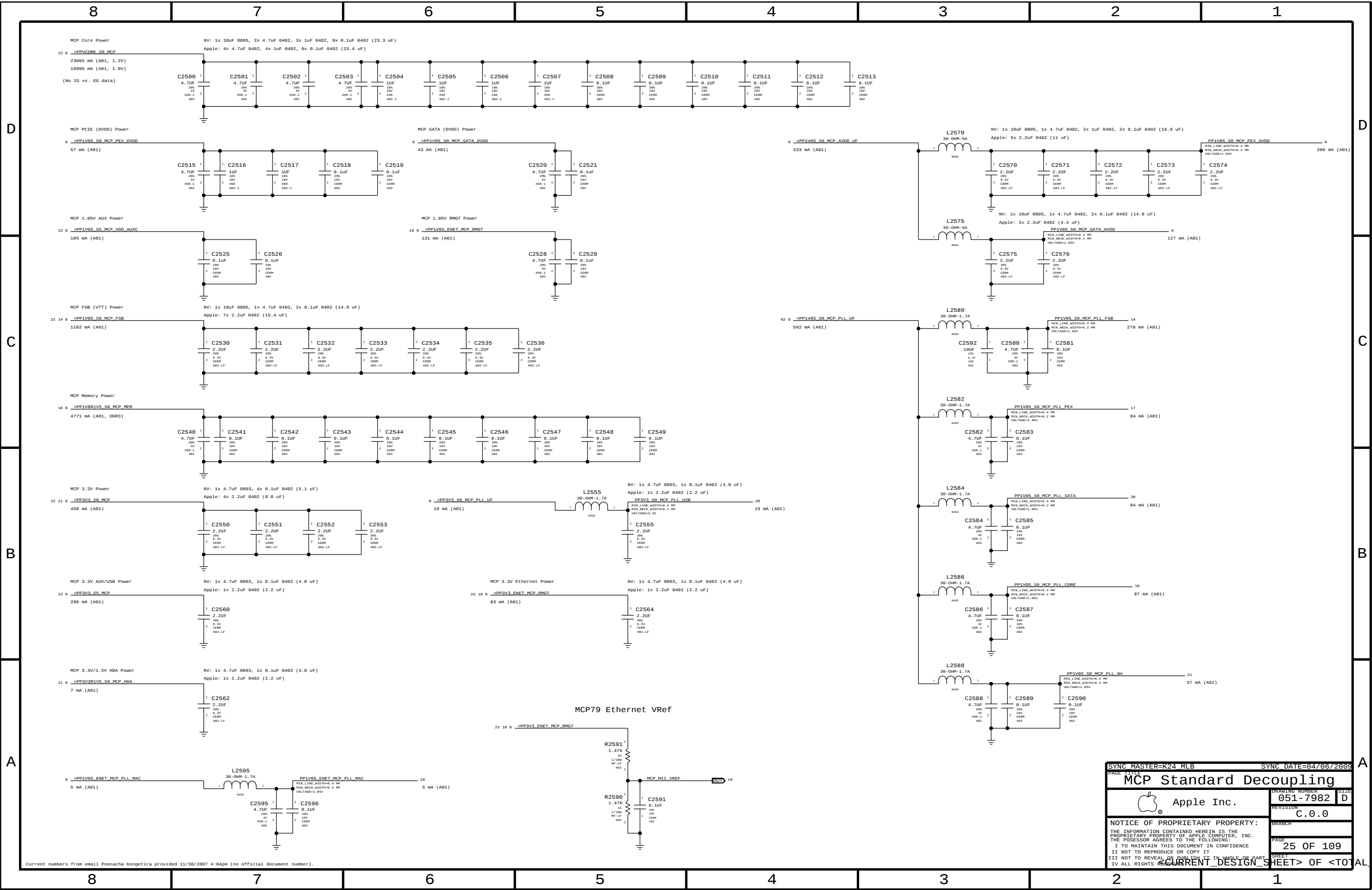
Frequency	SPI_D0	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

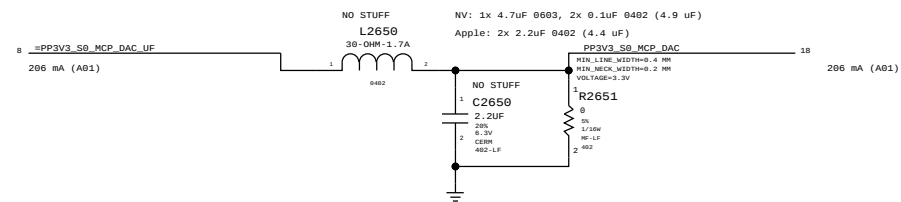
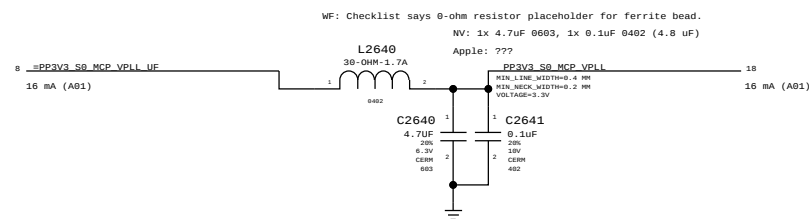
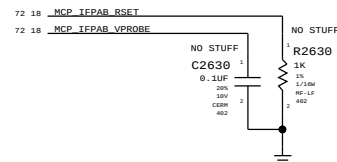
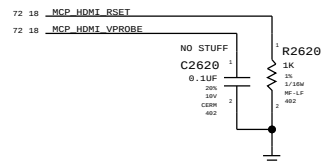
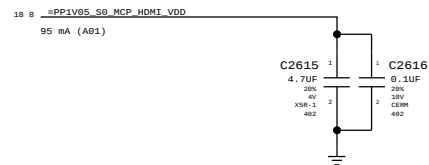
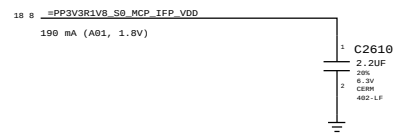
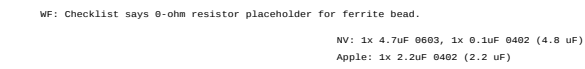
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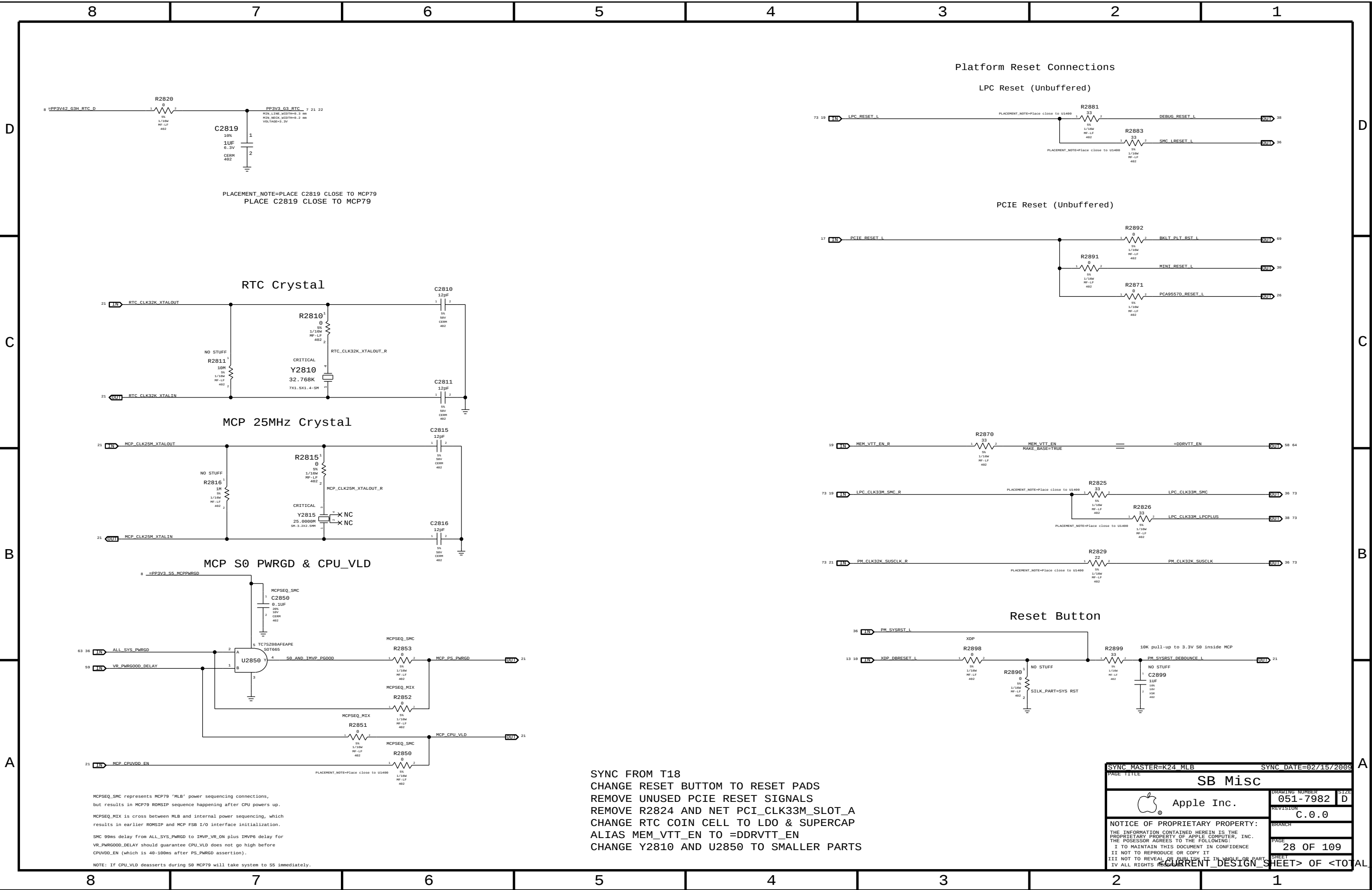


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SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDPC ROMS

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SYNCH MASTER=K24 MLB		SYNCH DATE=04/06/2009	
PAPER TITLE			
MCP Graphics Support			
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SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

Page Notes

Power aliases required by this page:

- #PP3V3_S3_VREFMRGN
- #PP3V3_S5_VREFMRGN
- #PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- `≡I2C_VREFDACS_SCL`
- `≡I2C_VREFDACS_SDA`
- `≡I2C_PCA9557D_SCL`
- `≡I2C_PCA9557D_SDA`

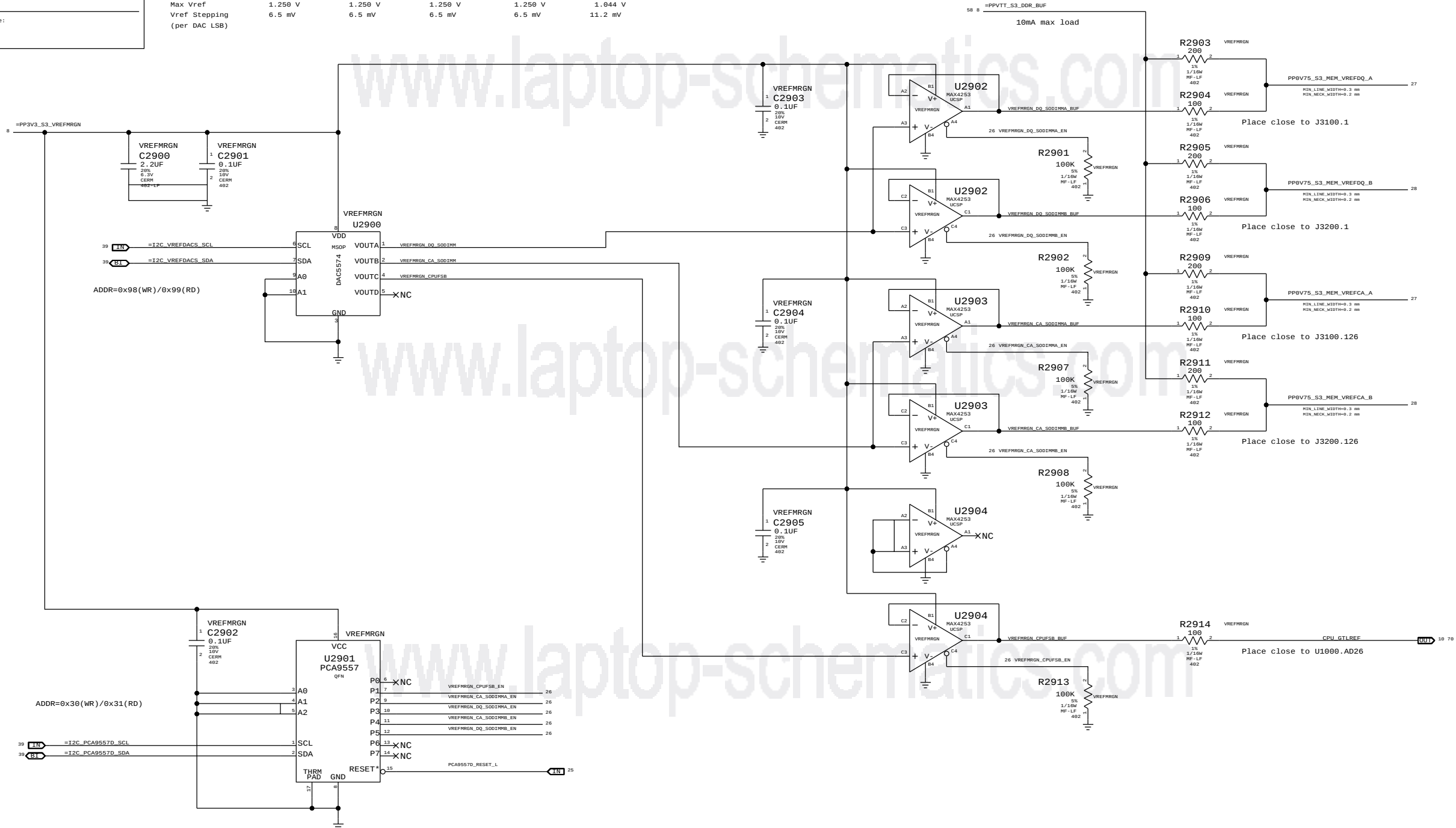
BOM options provided by this page:

VREFMRGN

NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM, 0, 5%, 0402, SM, LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM, 0, 5%, 0402, SM, LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM, 0, 5%, 0402, SM, LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM, 0, 5%, 0402, SM, LF	R2911	CRITICAL	NO_VREFMRGN

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

FSB/DDR3 Vref Margining



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1. *Journal of Management Studies*, 1996, 33, 1, 1-14.

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Page Notes

Power aliases required by this page:

-PP1V5_S0_MEM_B
-PP1V5_S3_MEM_B
-PP0V75_S0_MEM_VTT_B
-PP0V75_S3_MEM_VTT_B
-PP0V75_S0_MEM_SDA (2.5 - 3.3V)
-PP0V75_S3_MEM_SDA

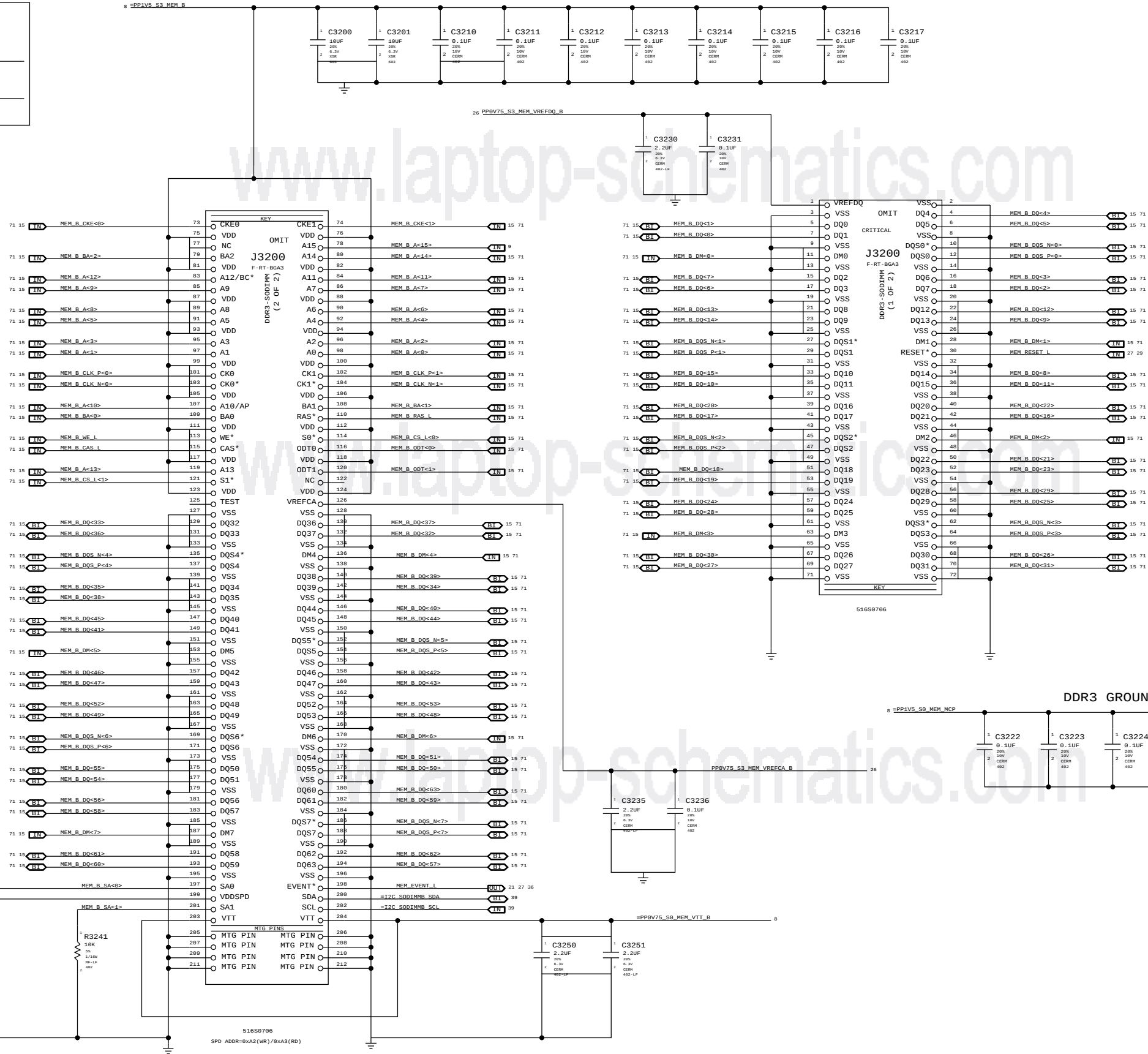
Signal aliases required by this page:

-I2C_S0D1MMB_SCL
-I2C_S0D1MMB_SDA

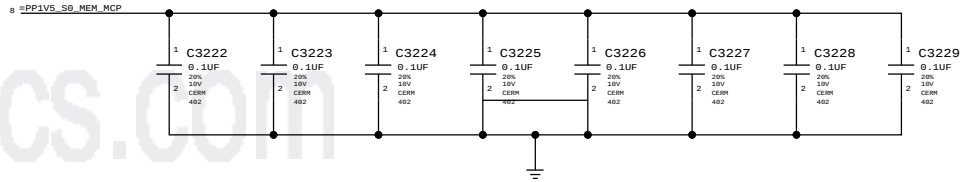
ROM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

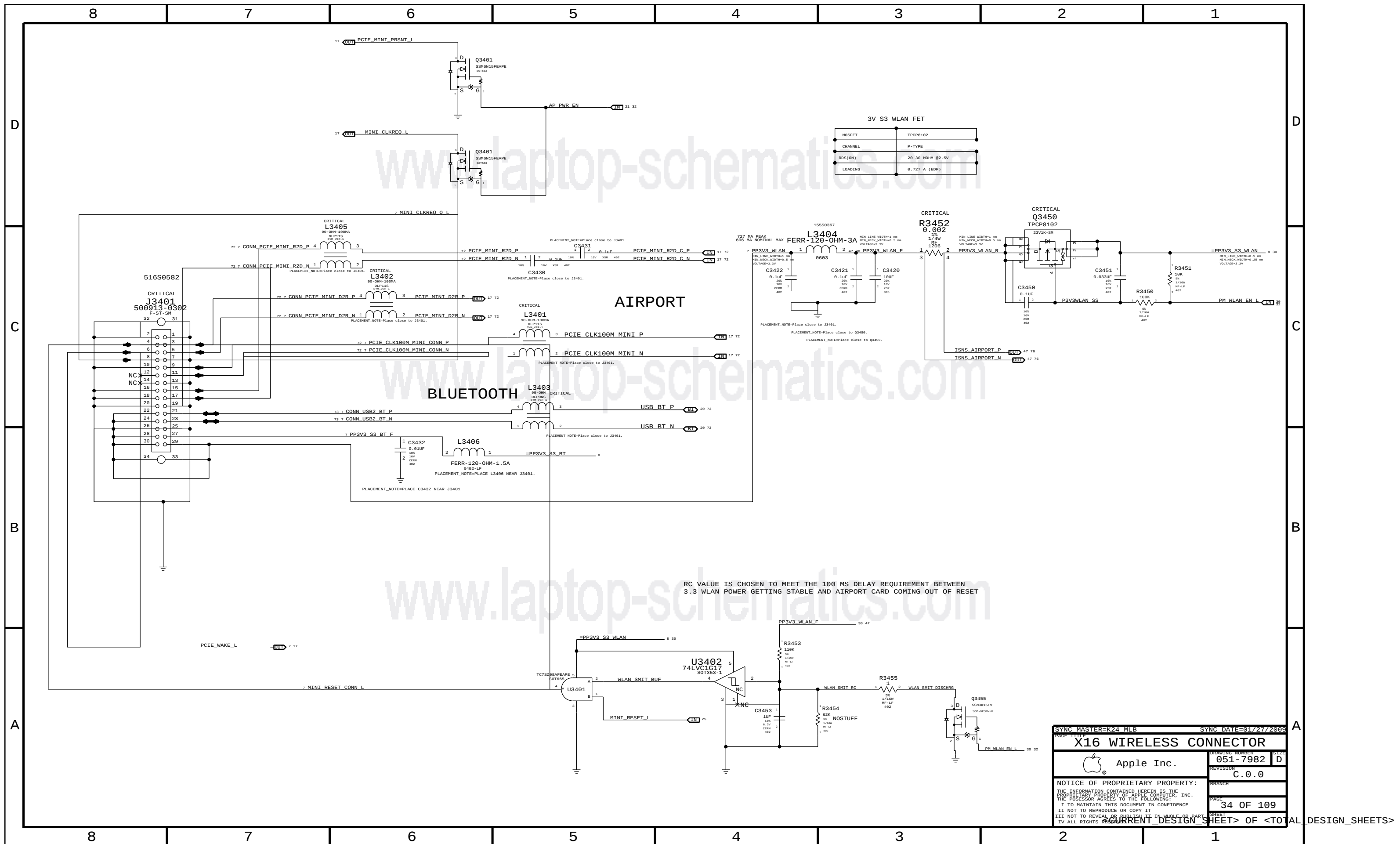


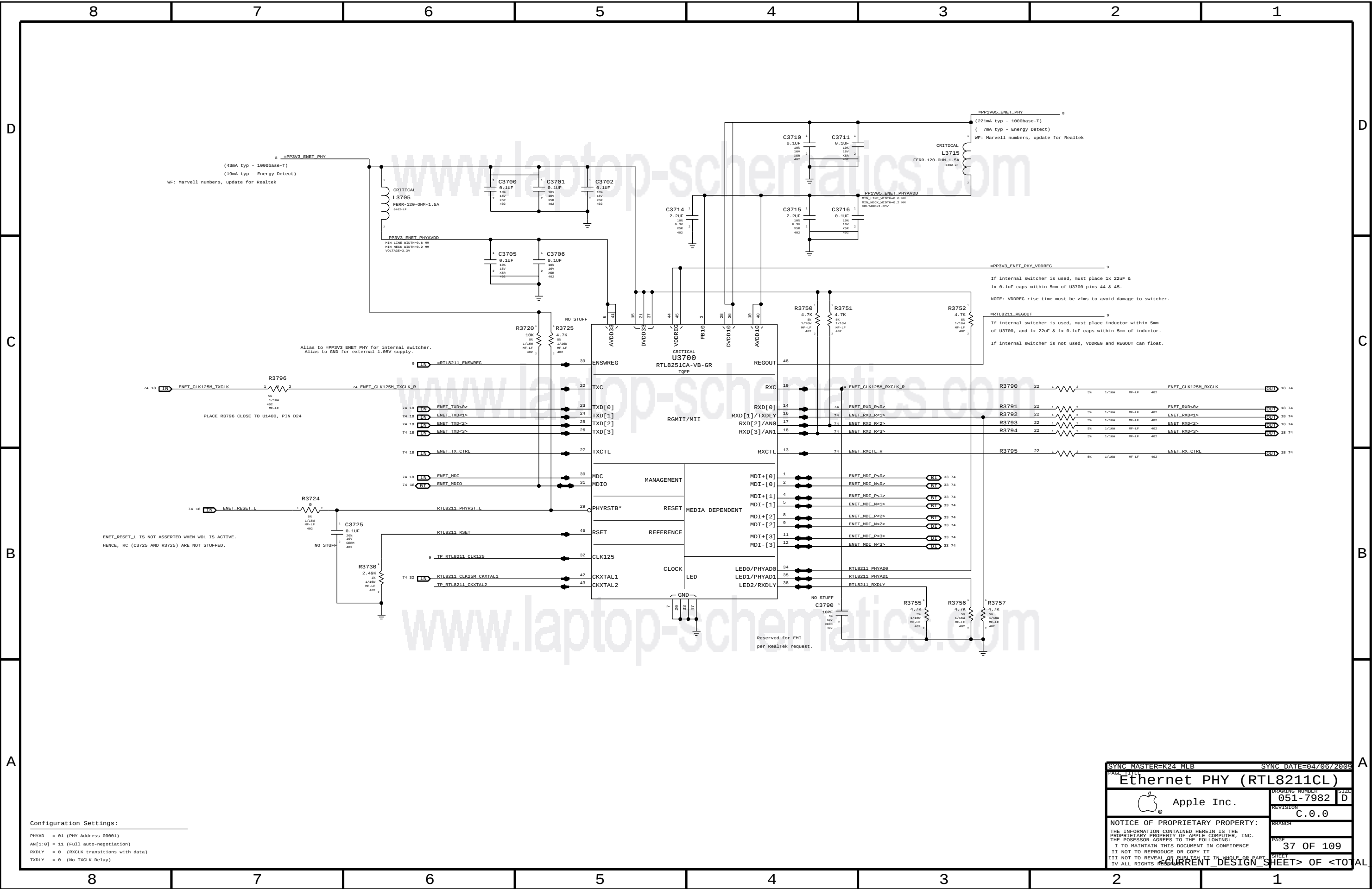
DDR3 GROUND RETURN CAPS (MCP SIDE)



"Expansion" (bottom) slot

SYNC MASTER=K24 MLB		SYNC DATE=02/05/2009	
PAGE TITLE			
DDR3 S0-DIMM Connector B			
DRAWING NUMBER		SIZE	
051-7982		D	
REVISION		C.0.0	
BRANCH		PAGE	
		32 OF 109	
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D

C

B

A

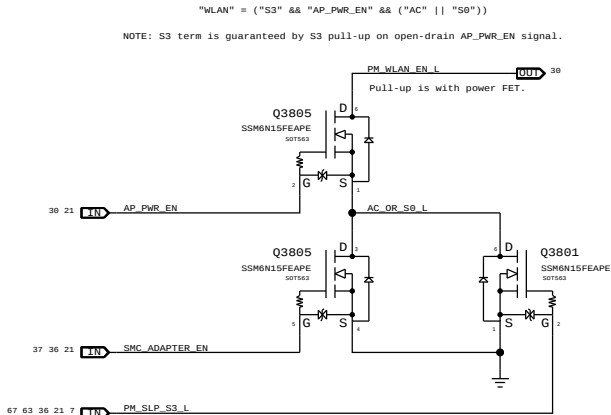
D

C

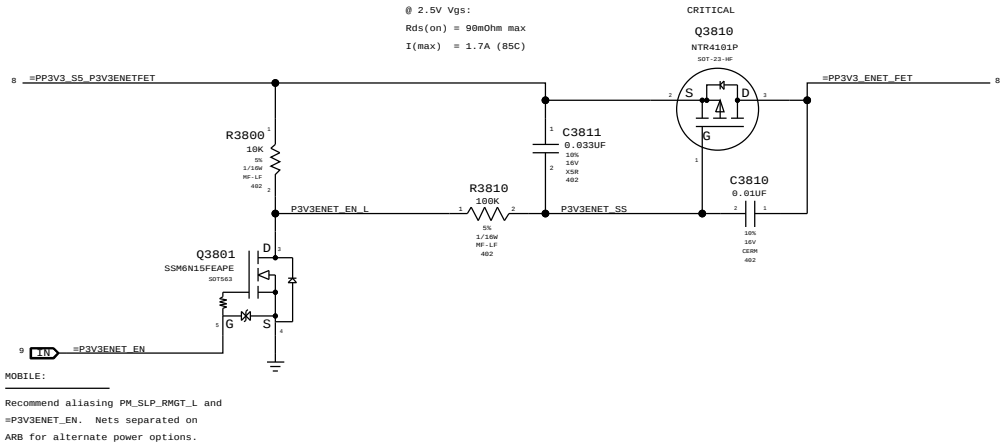
B

A

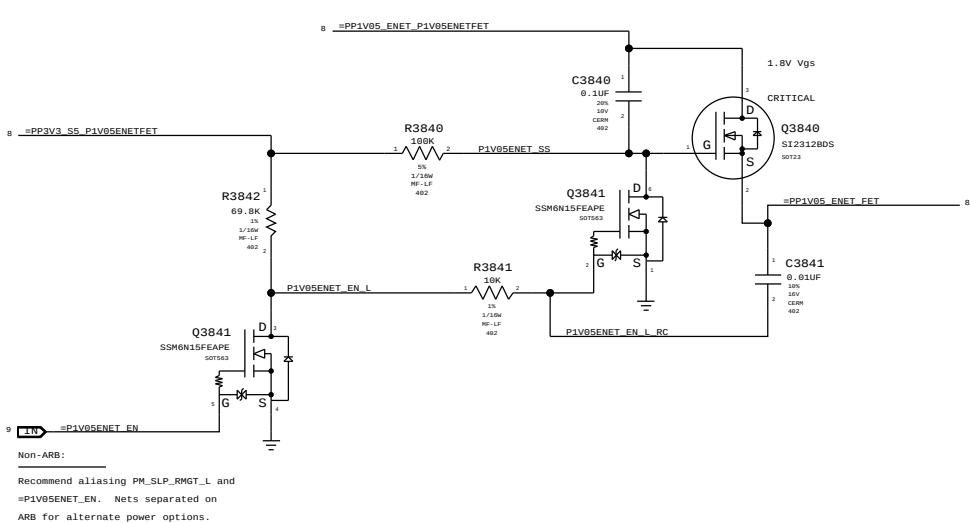
WLAN Enable Generation



3.3V ENET FET

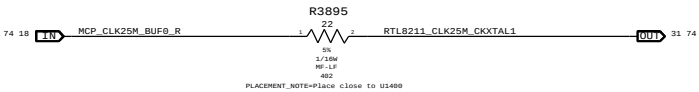


1.05V ENET FET



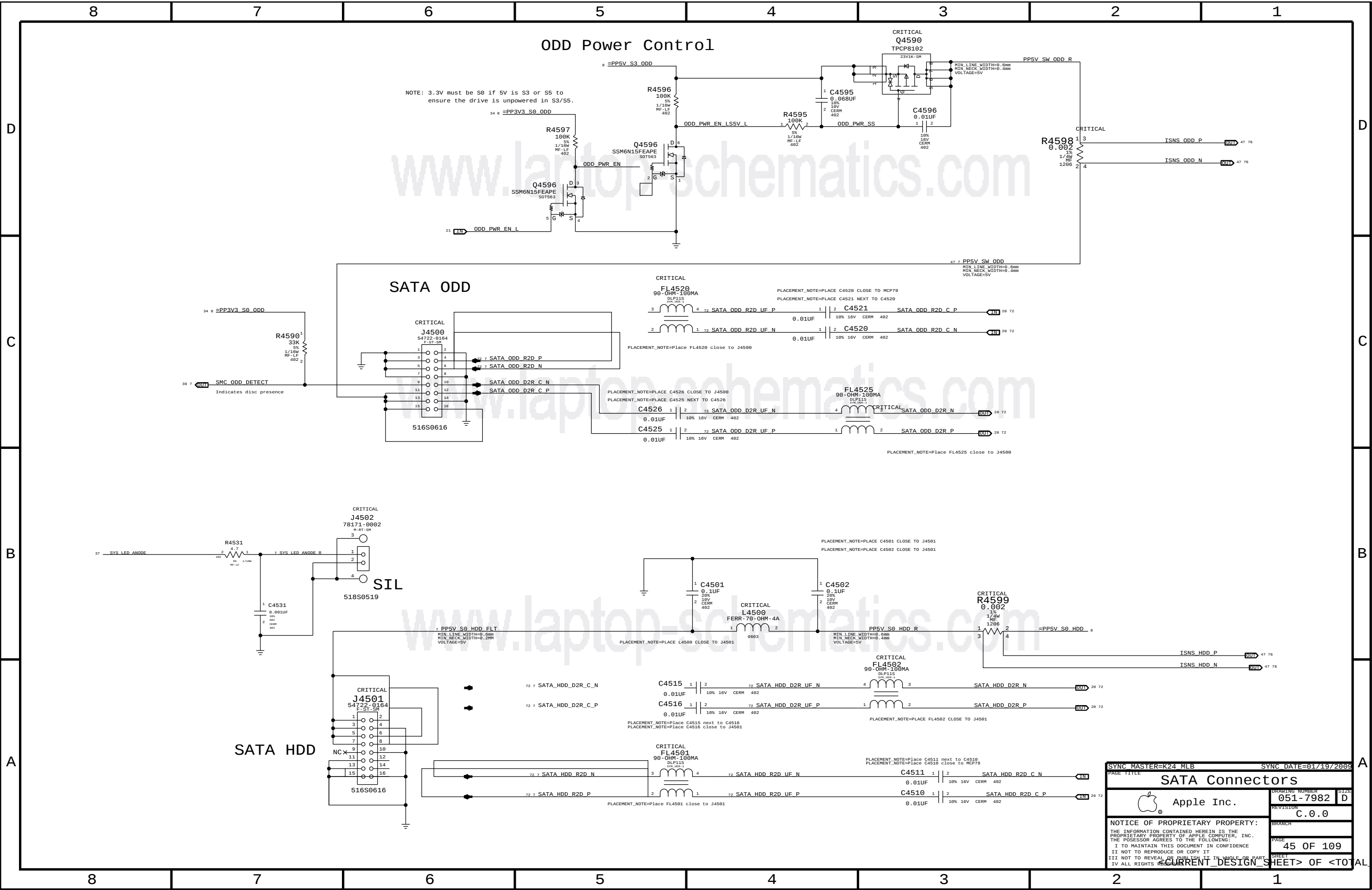
RTL8211 25MHz Clock

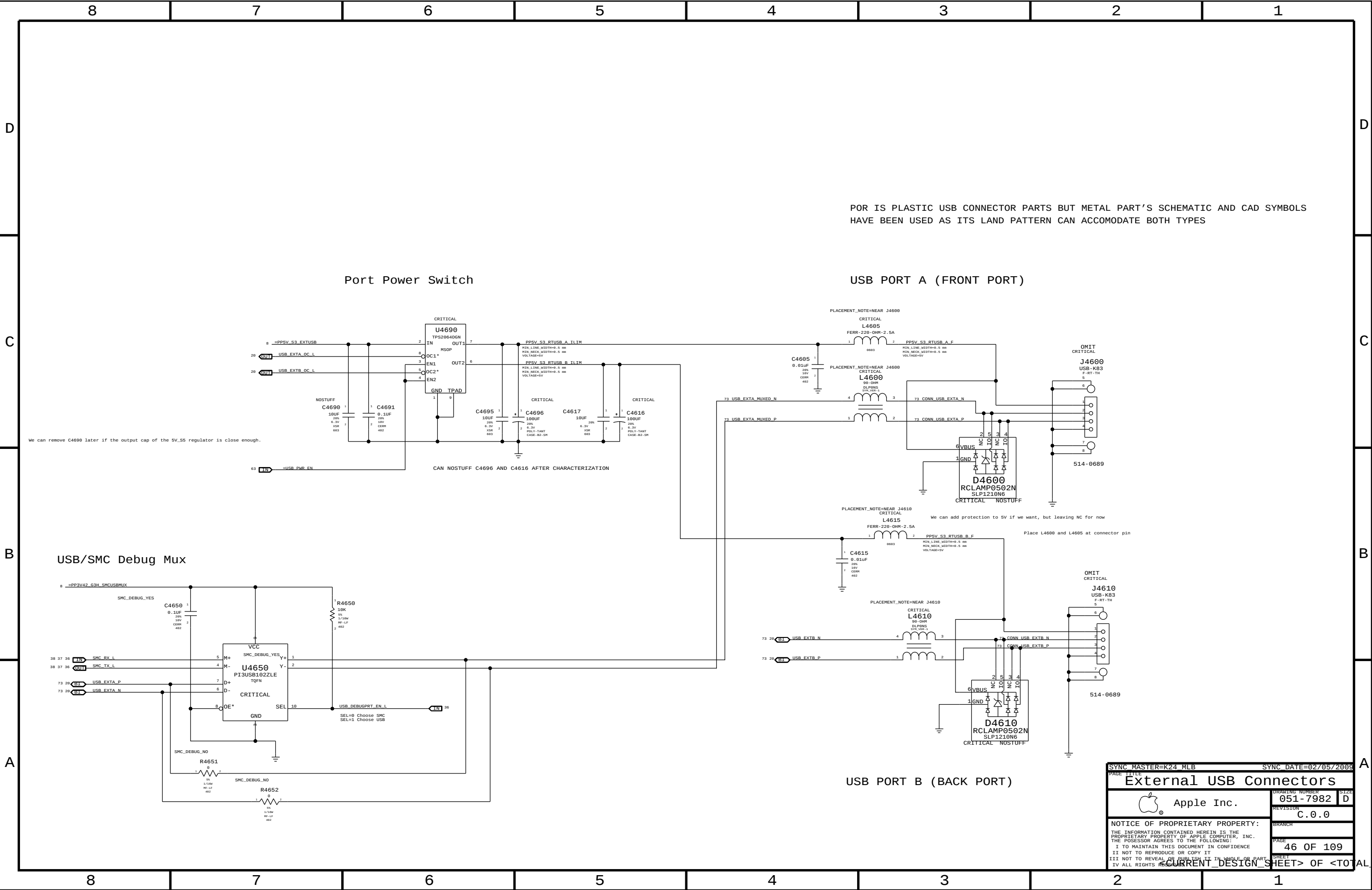
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

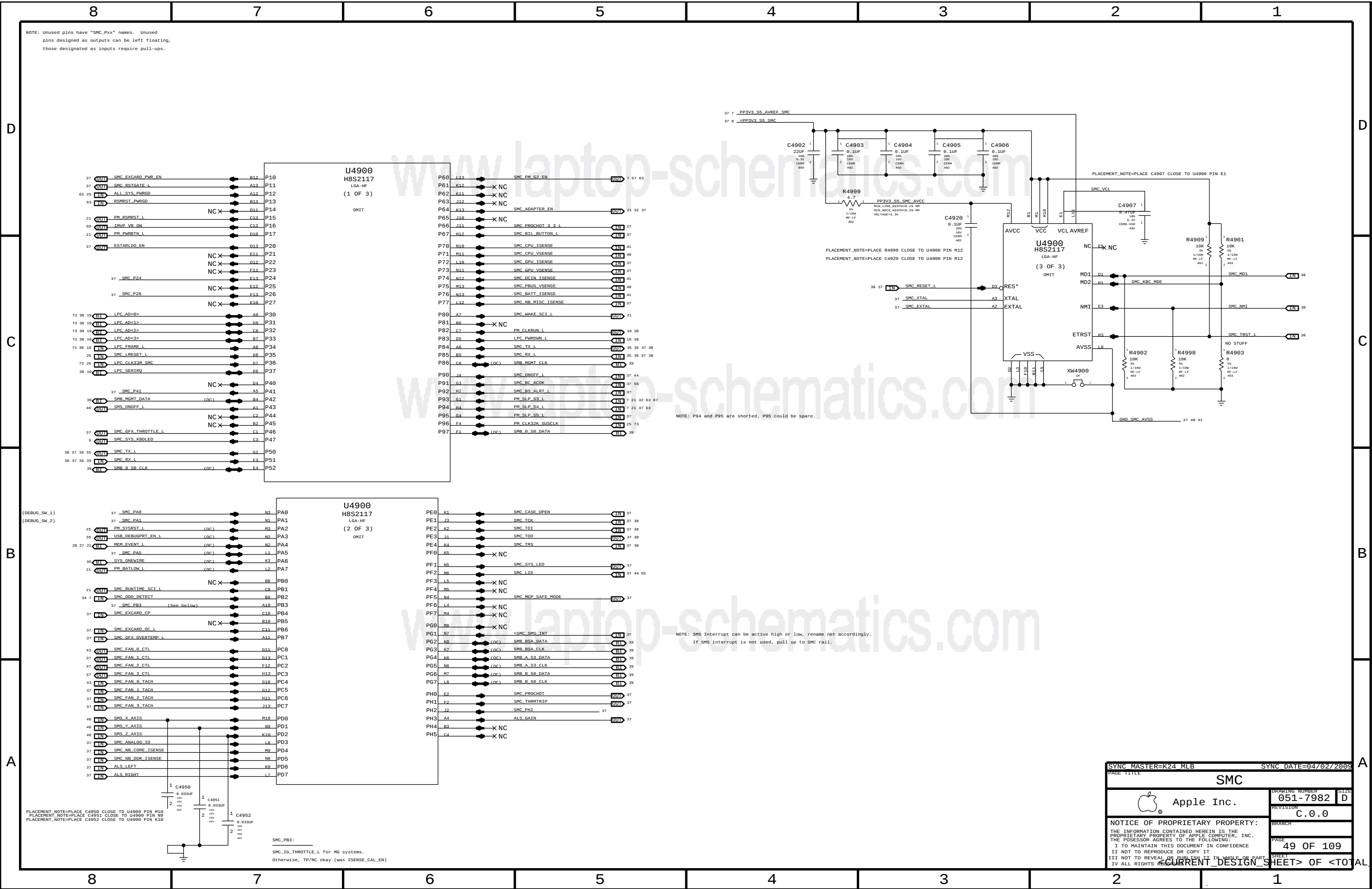


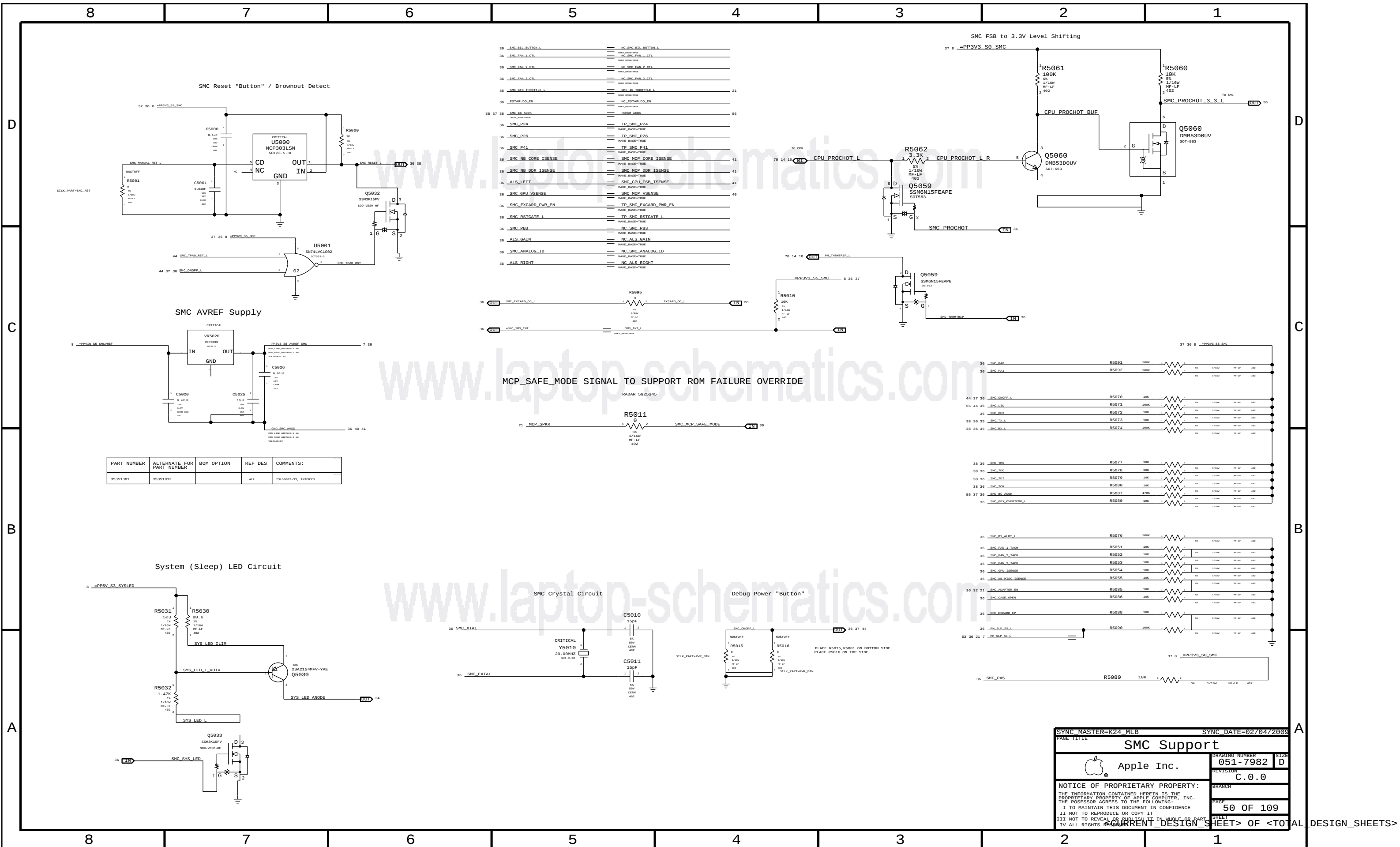
SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE Ethernet & AirPort Support			
DRAWING NUMBER 051-7982		SIZE D	
REVISION C.0.0		BRANCH	
PAGE 38 OF 109		SHEET	
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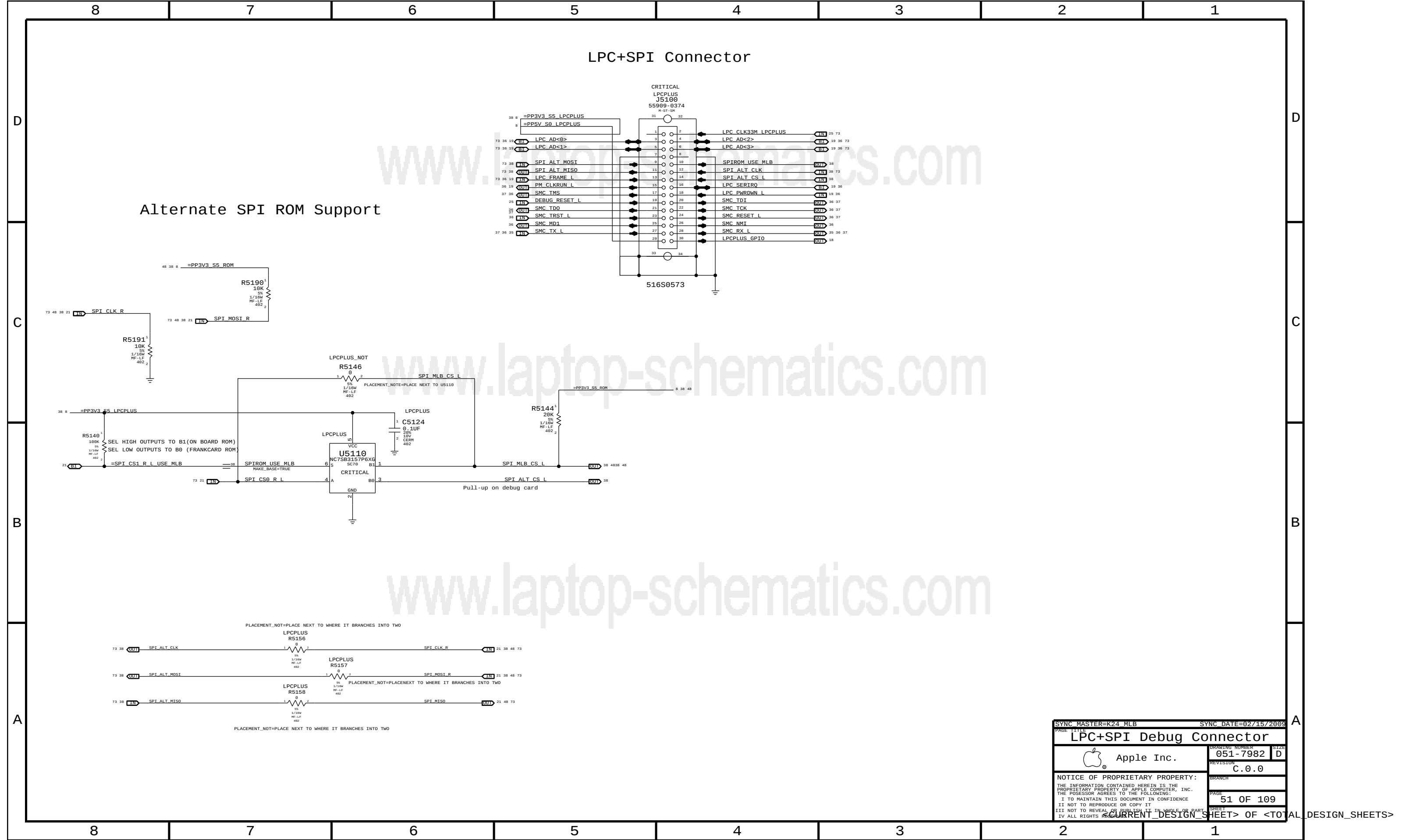
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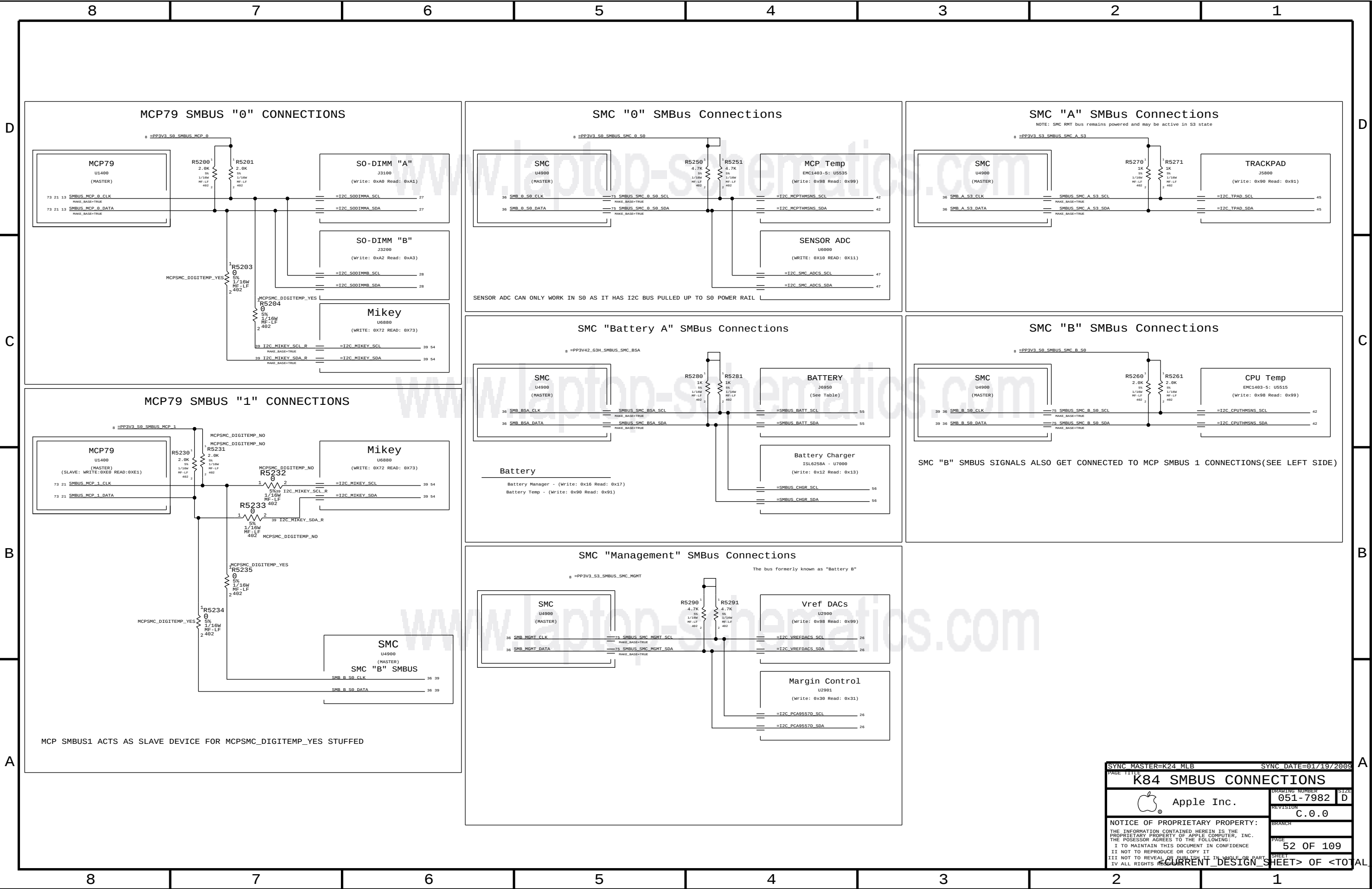


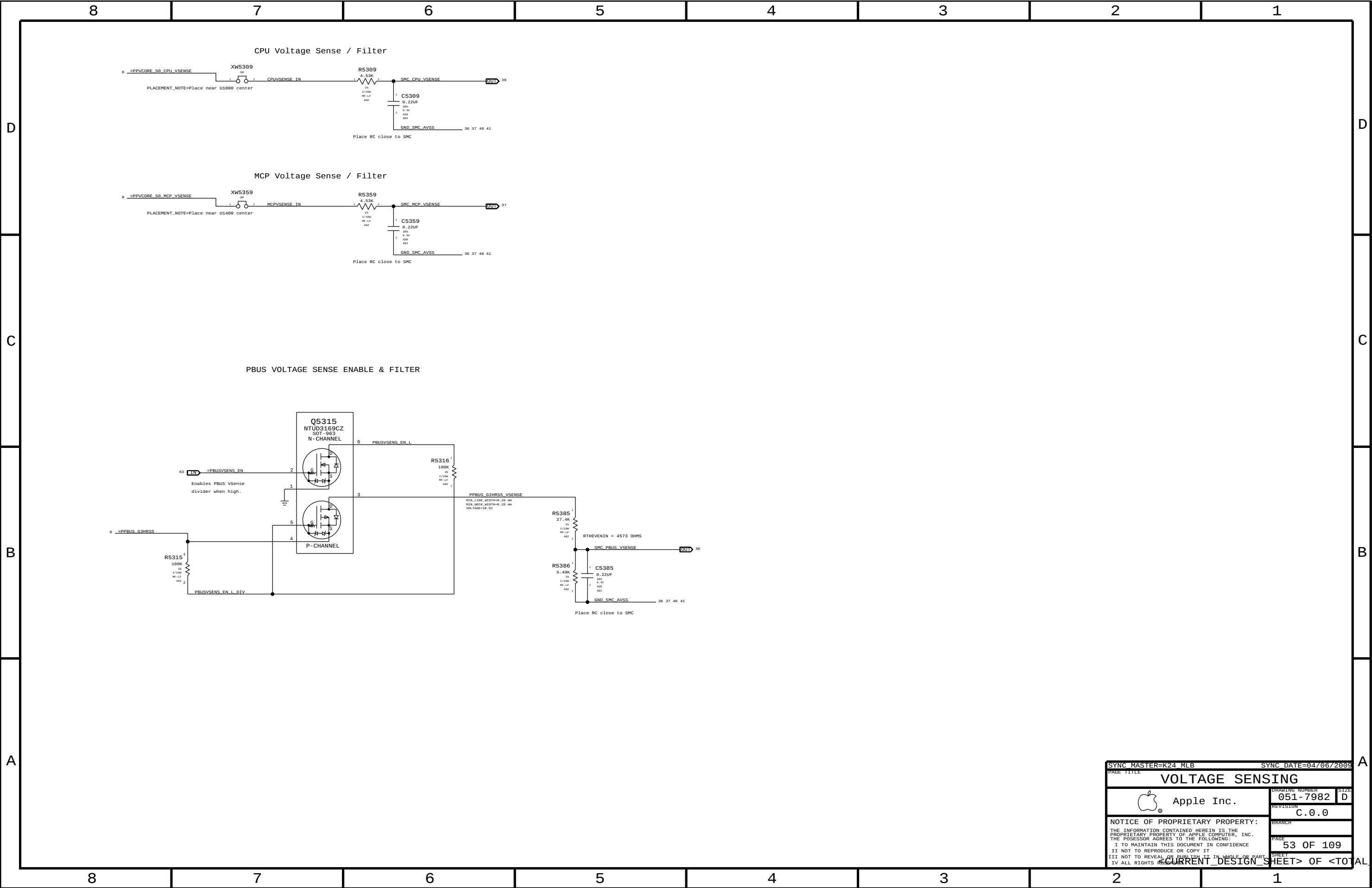




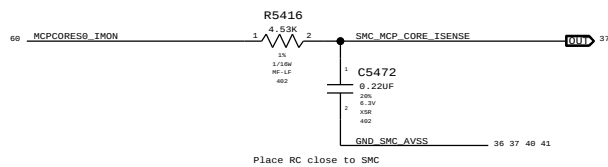




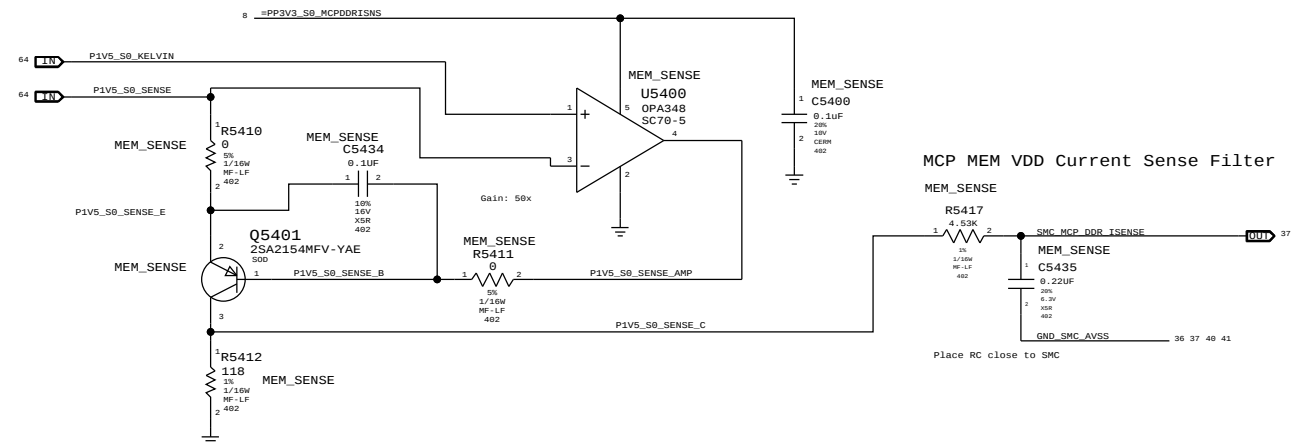




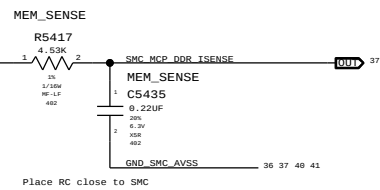
SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
VOLTAGE SENSING			
 Apple Inc.		DRAWING NUMBER	051-7982
		REVISION	C.0.0
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		PAGE	53 OF 109
CURRENT DESIGN SHEET>		SHEET> OF <TOTAL>	



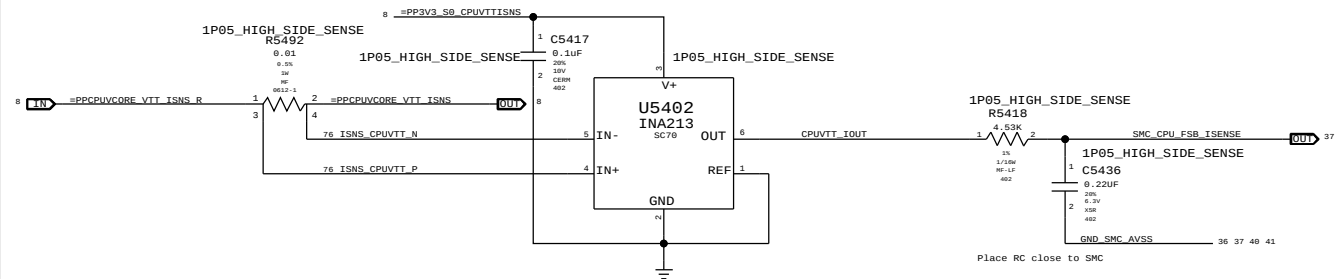
MCP MEM VDD Current Sense



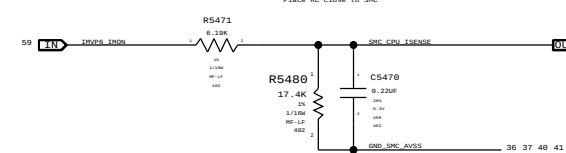
MCP MEM VDD Current Sense Filter



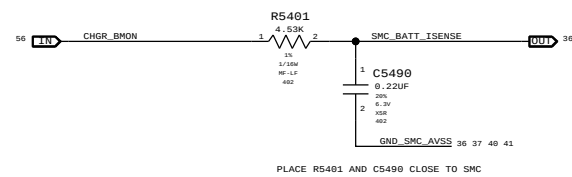
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



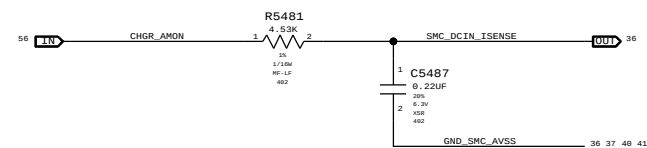
CPU VCore Load Side Current Sense / Filter

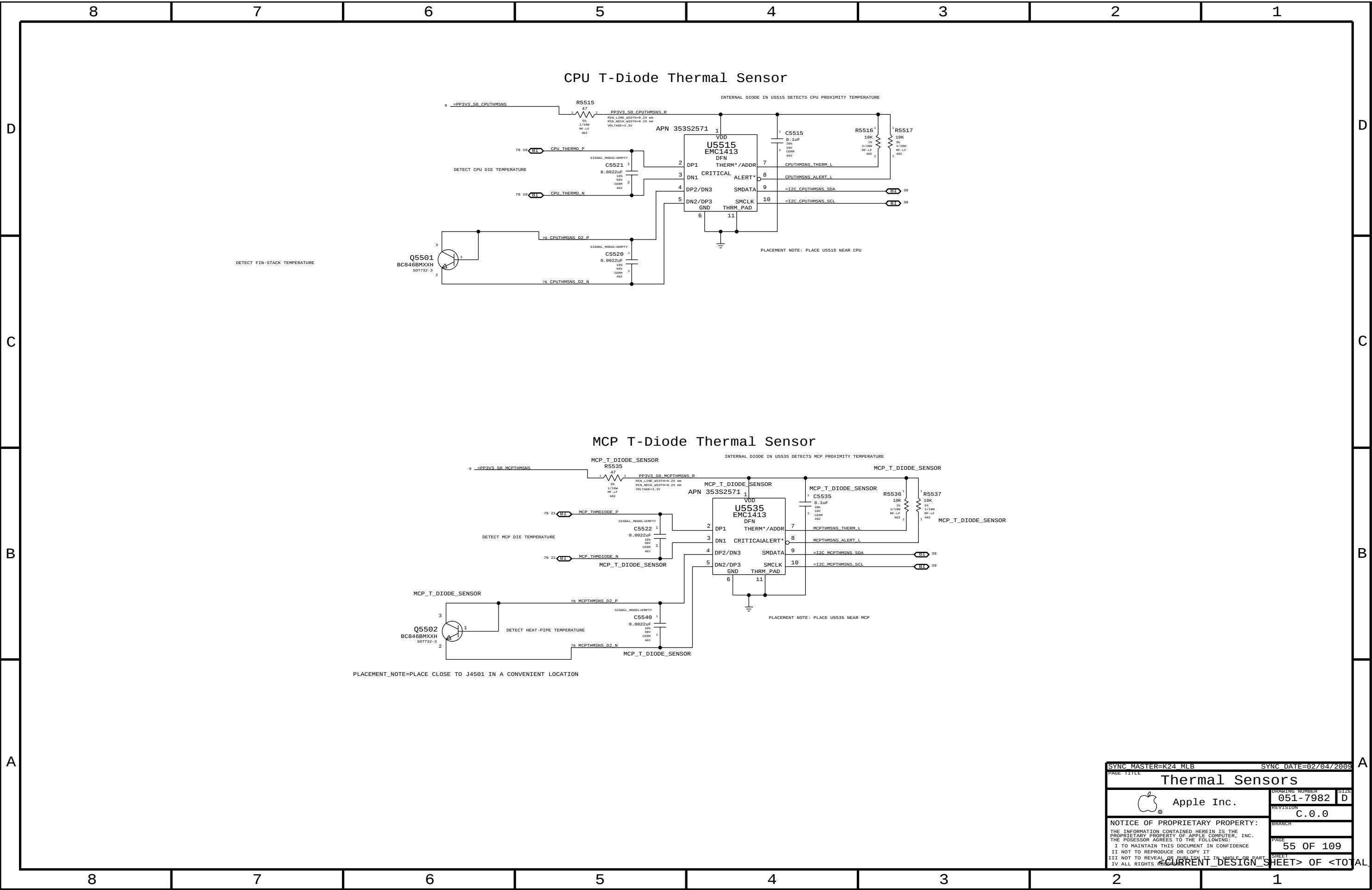


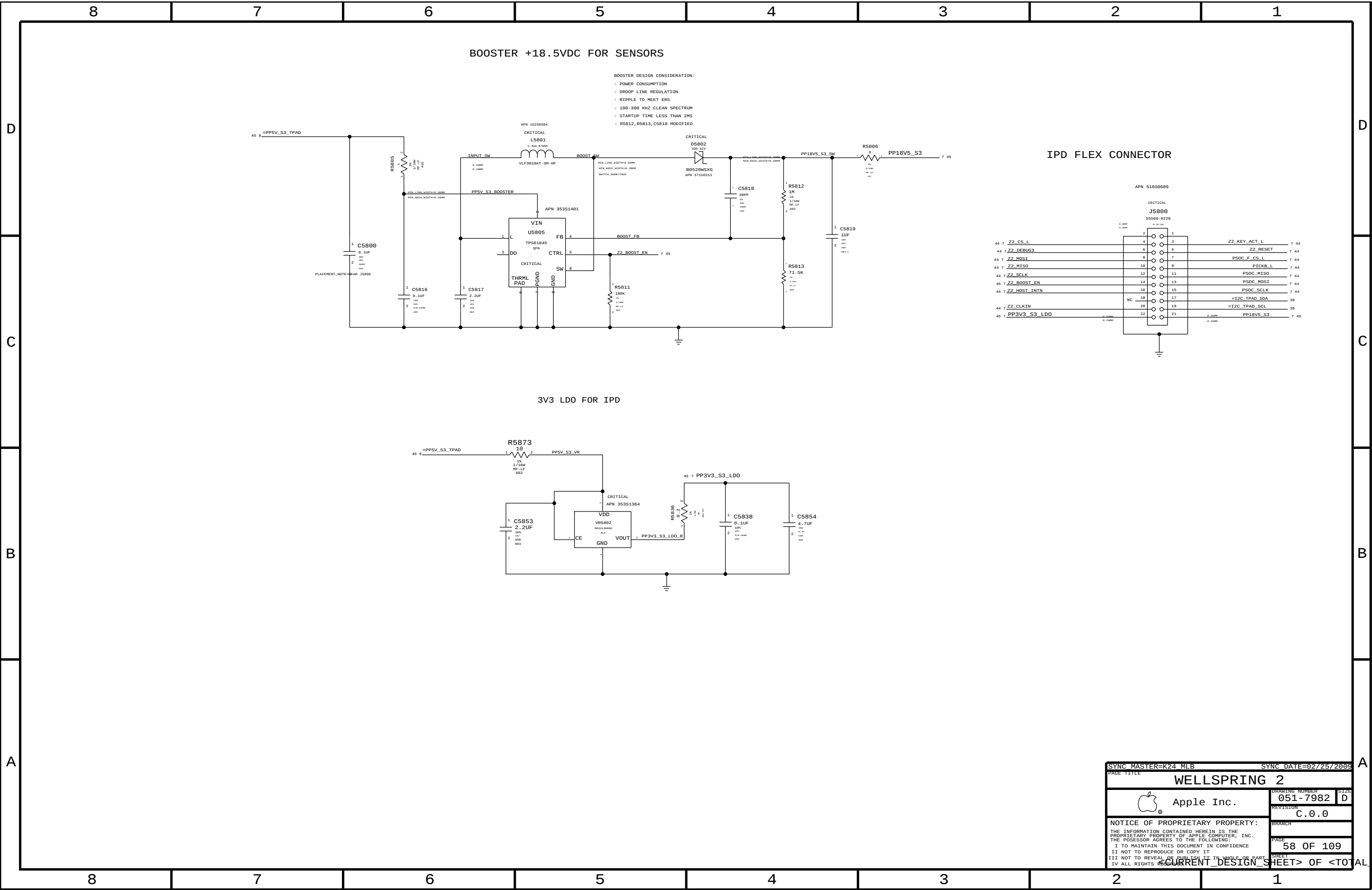
DC-IN (BMON) CURRENT SENSE

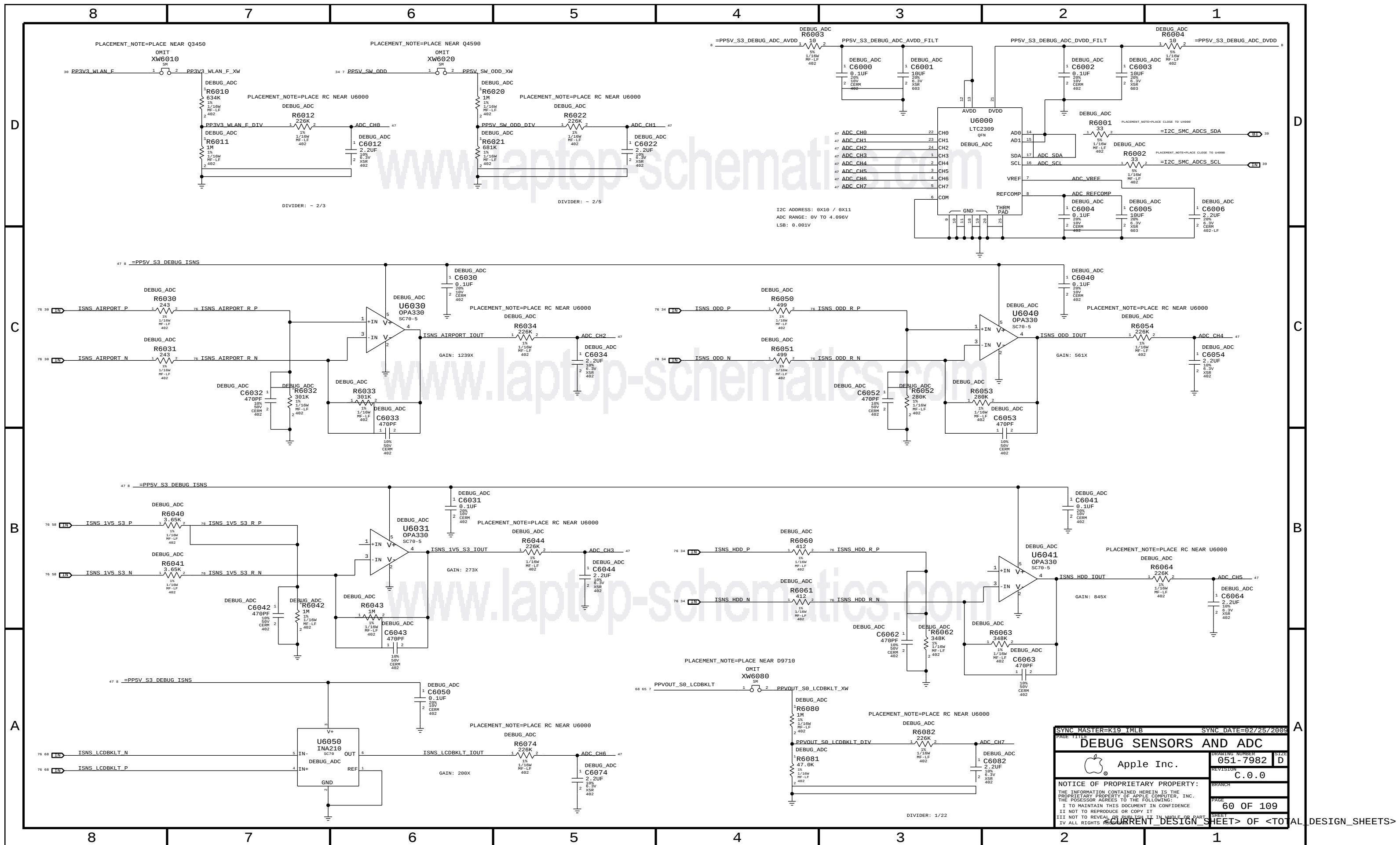


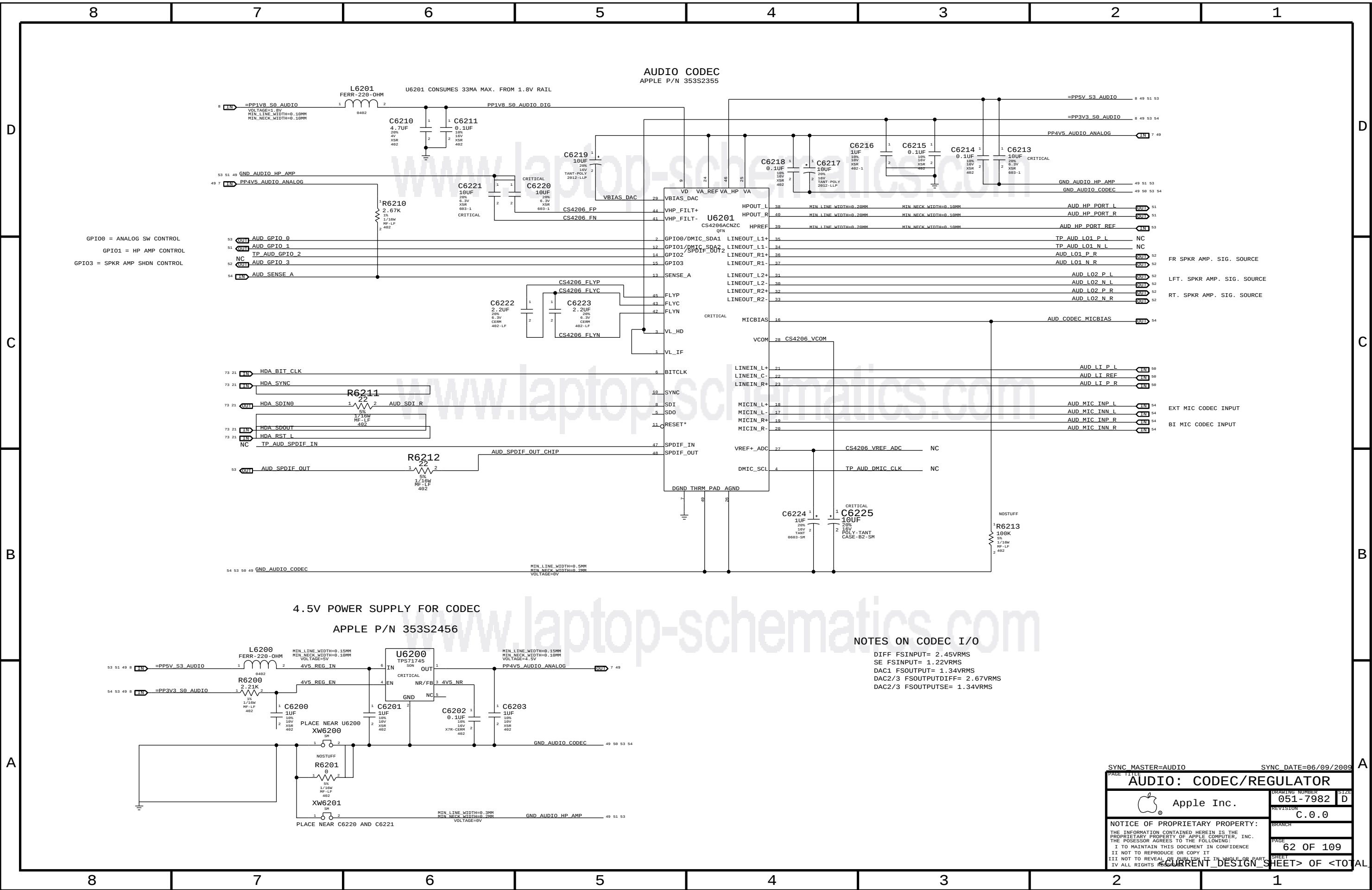
DC-IN (AMON) CURRENT SENSE



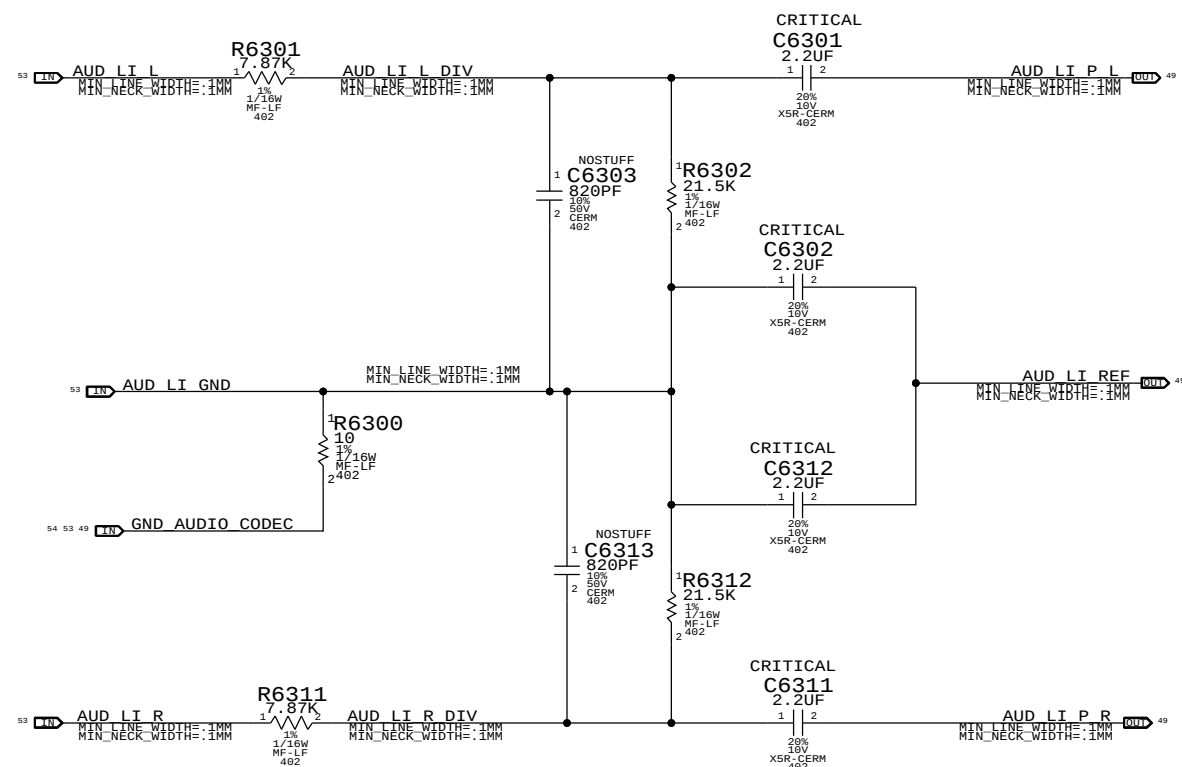




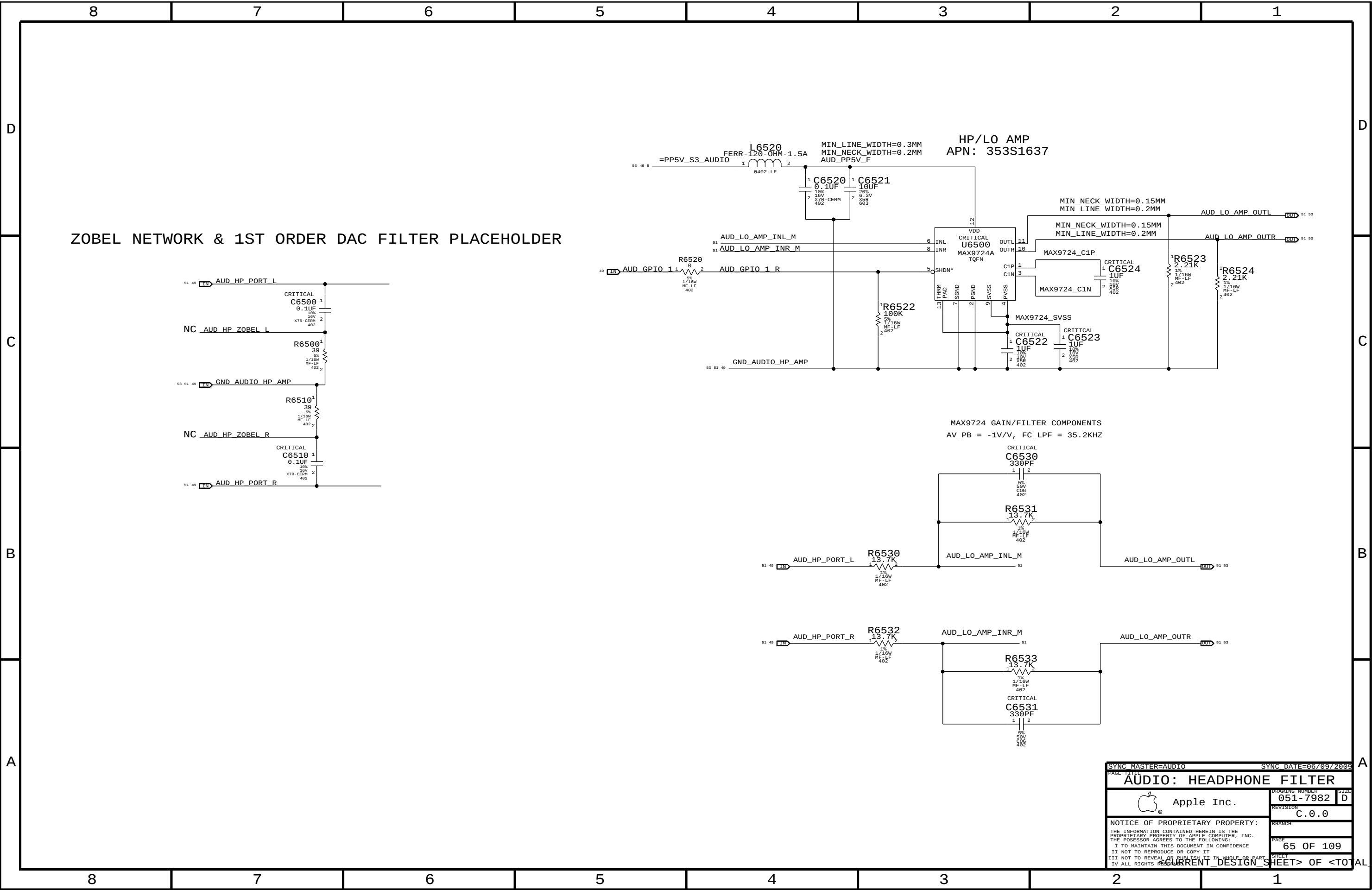


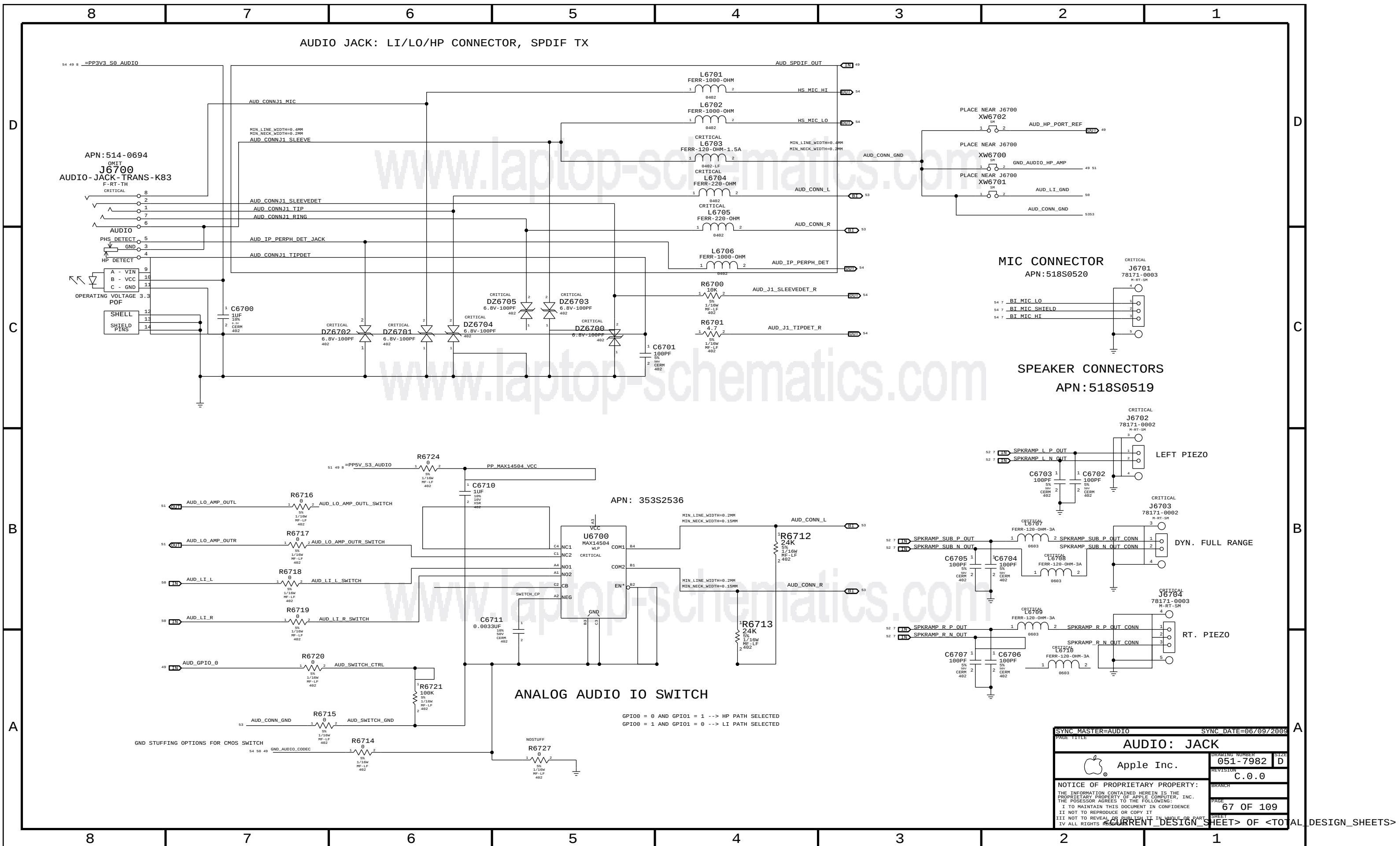


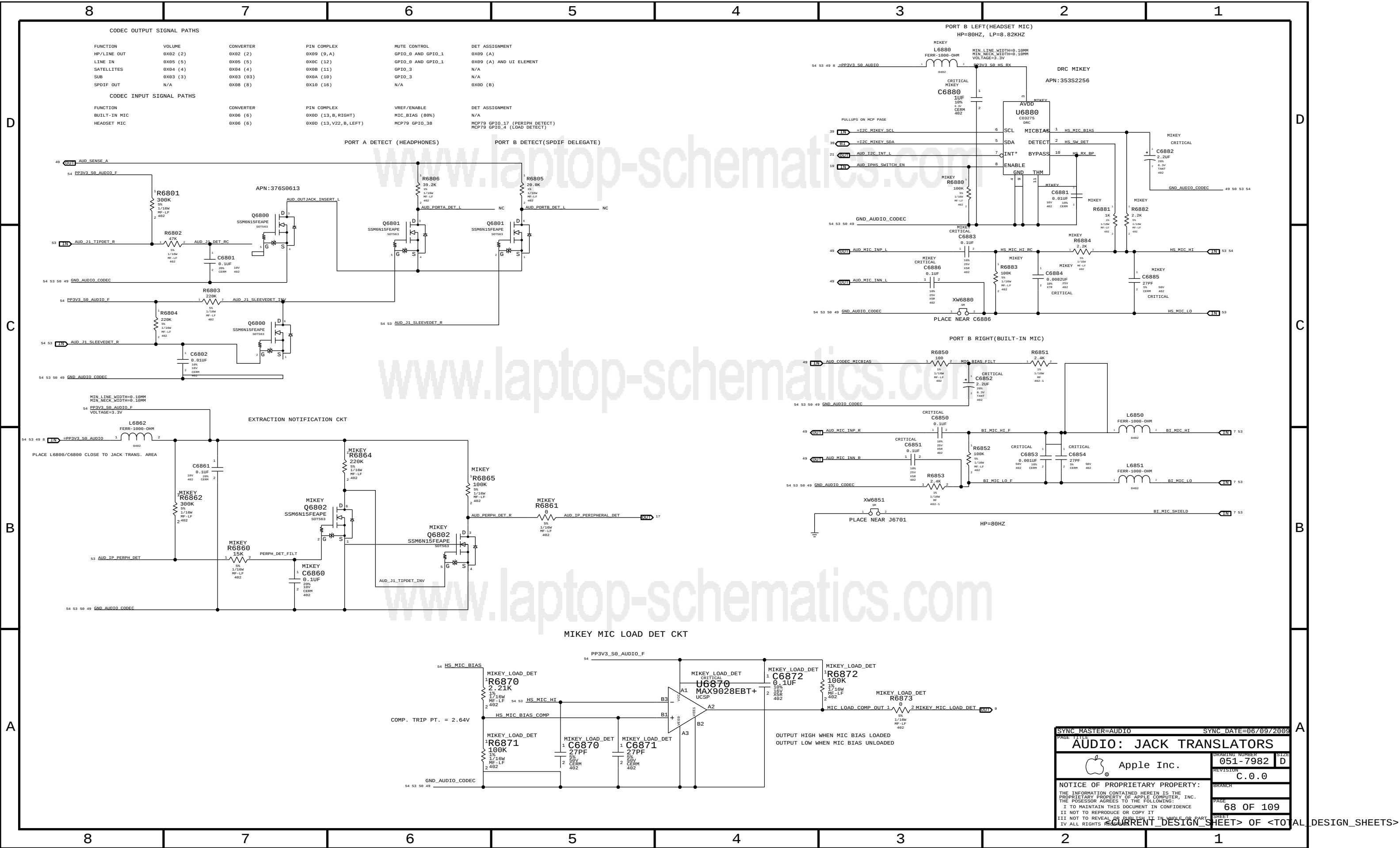
```
CODEC_RIN = 20K OHMS
NET_RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC_VIN = 1.14 VRMS
```



PAGE TITLE		DRAWING NUMBER		SHEET	
AUDIO: LINE INPUT FILTER		051-7982		D	
 Apple Inc.		REVISION		C.0.0	
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SYNC MASTER=AUDIO SYNC DATE=06/09/2009

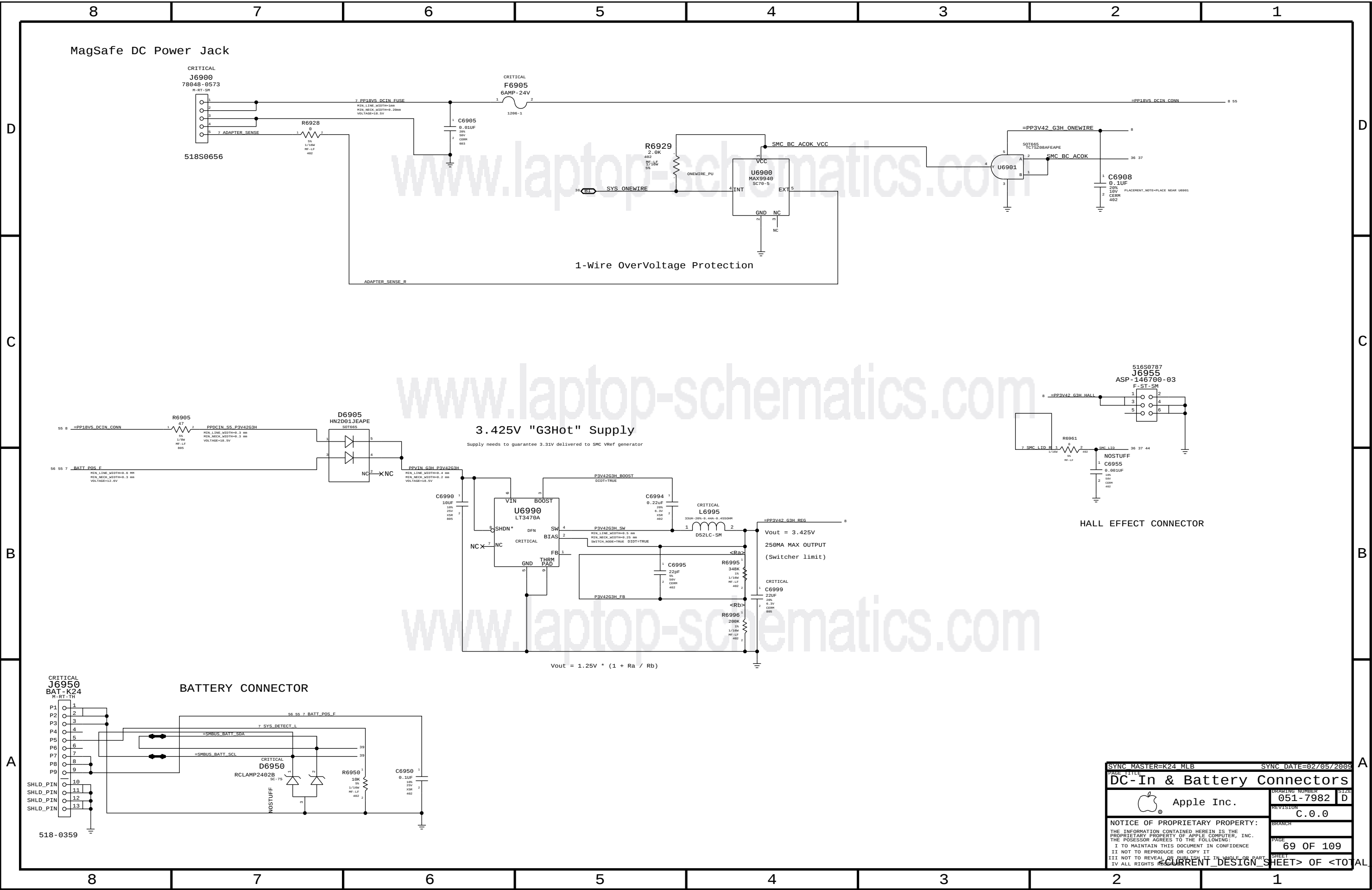
AUDIO: JACK TRANSLATORS

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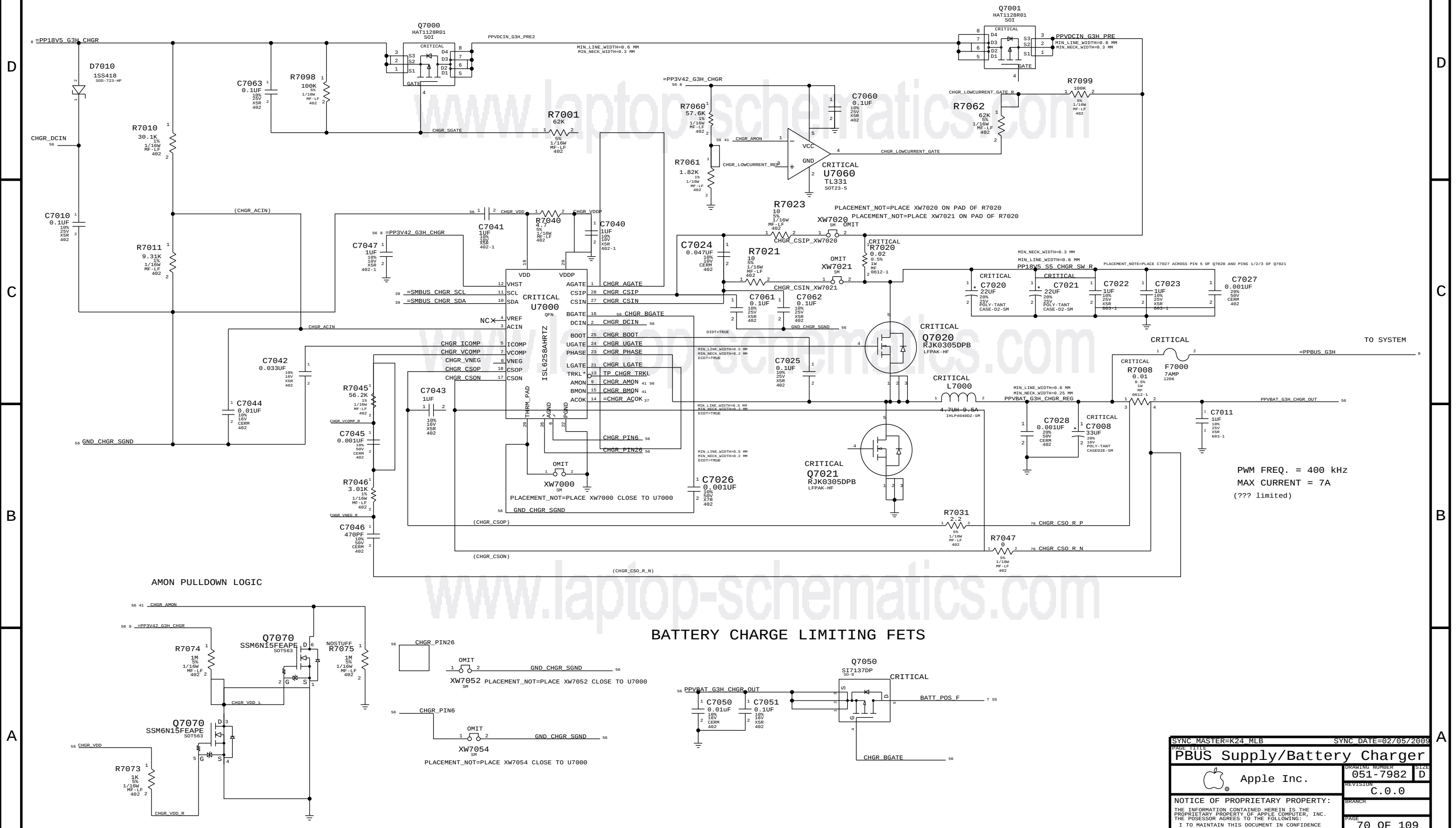
DRAWING NUMBER: 051-7982
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PAGE: 68 OF 109
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PAGE TITLE		SYNC MASTER=K24 MLB		SYNC DATE=02/05/2009	
DC-In & Battery Connectors		DRAWING NUMBER		051-7982 D	
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PBUS SUPPLY / BATTERY CHARGER



SYNC MASTER=K24 MLB

SYNC DATE=02/05/2009

PAGE TITLE

PBUS Supply/Battery Charger

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051-7982 D

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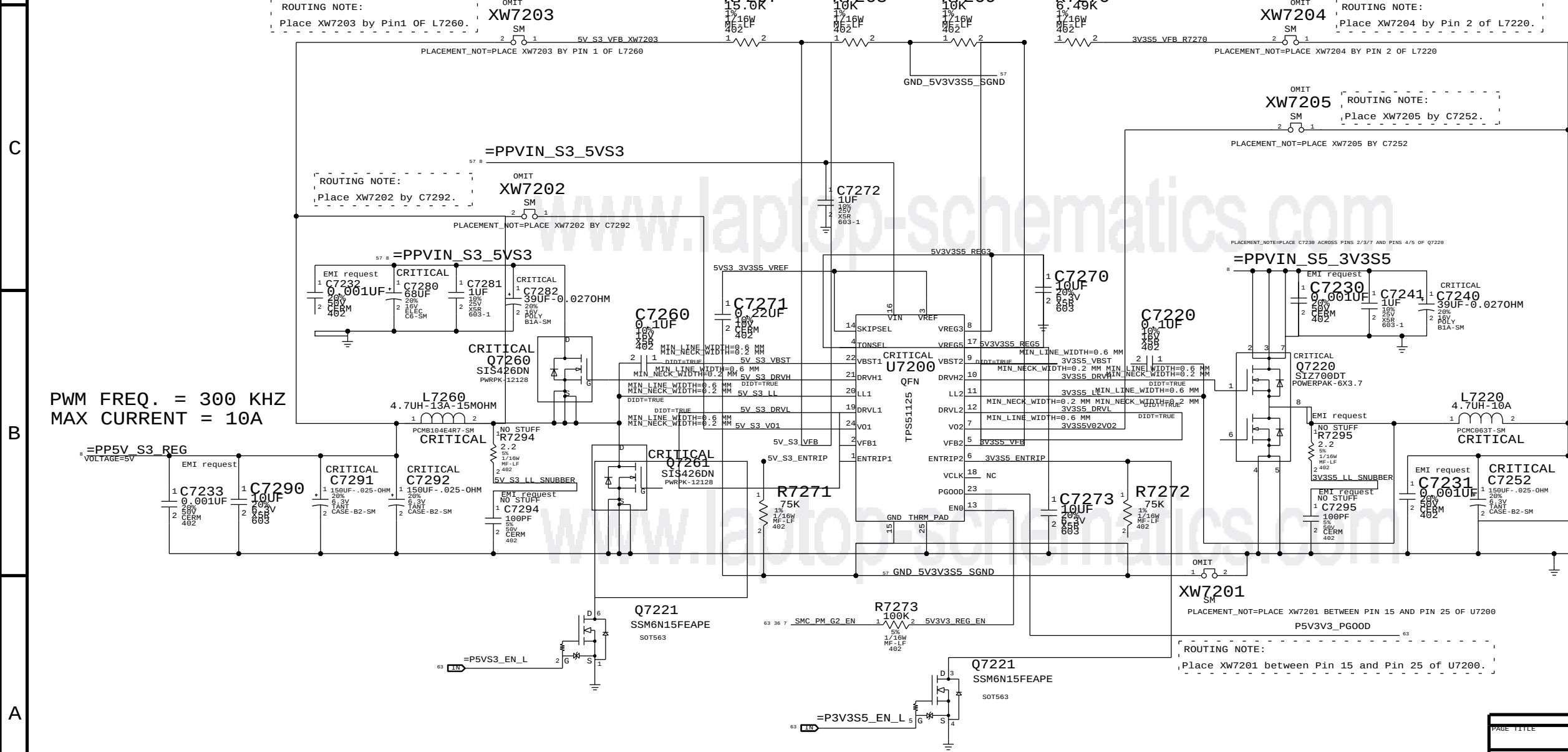
5V S3/3.3V S5 POWER SUPPLY

$$V_{OUT} = (2 * RA / RB) + 2$$
$$V_{OUT} = (2 * RC / RD) + 2$$

PWM FREQ. = 300 KHZ
MAX CURRENT = 10A

PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

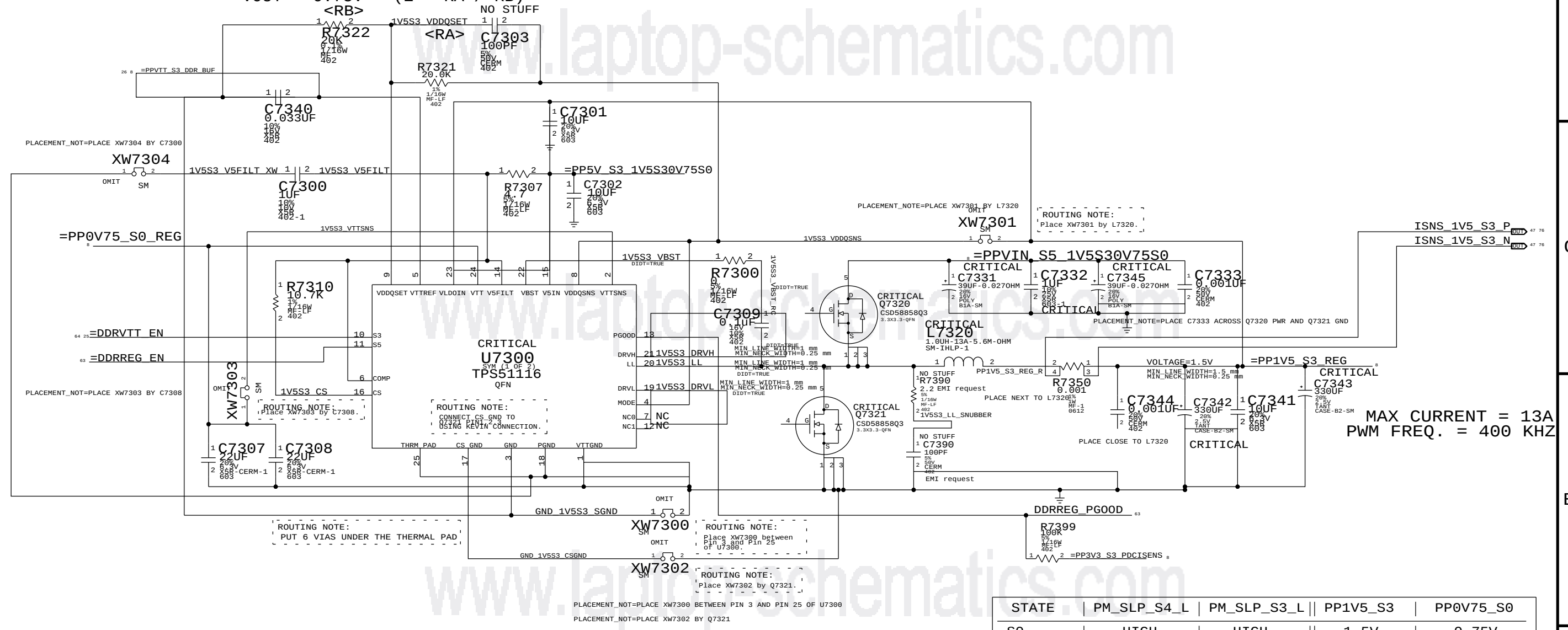
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5V/3.3V SUPPLY	
Apple Inc.	DRAWING NUMBER
	051-7982
	REVISION
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PAGE	SHEET
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SEPERATED MASTER PG000 FOR BOTH 5V AND 3V3.

1.5V/0.75V(DDR3) POWER SUPPLY

$$V_{OUT} = 0.75V * (1 + \frac{R_A}{R_B})$$



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

1.5V/0.75V DDR3 SUPPLY

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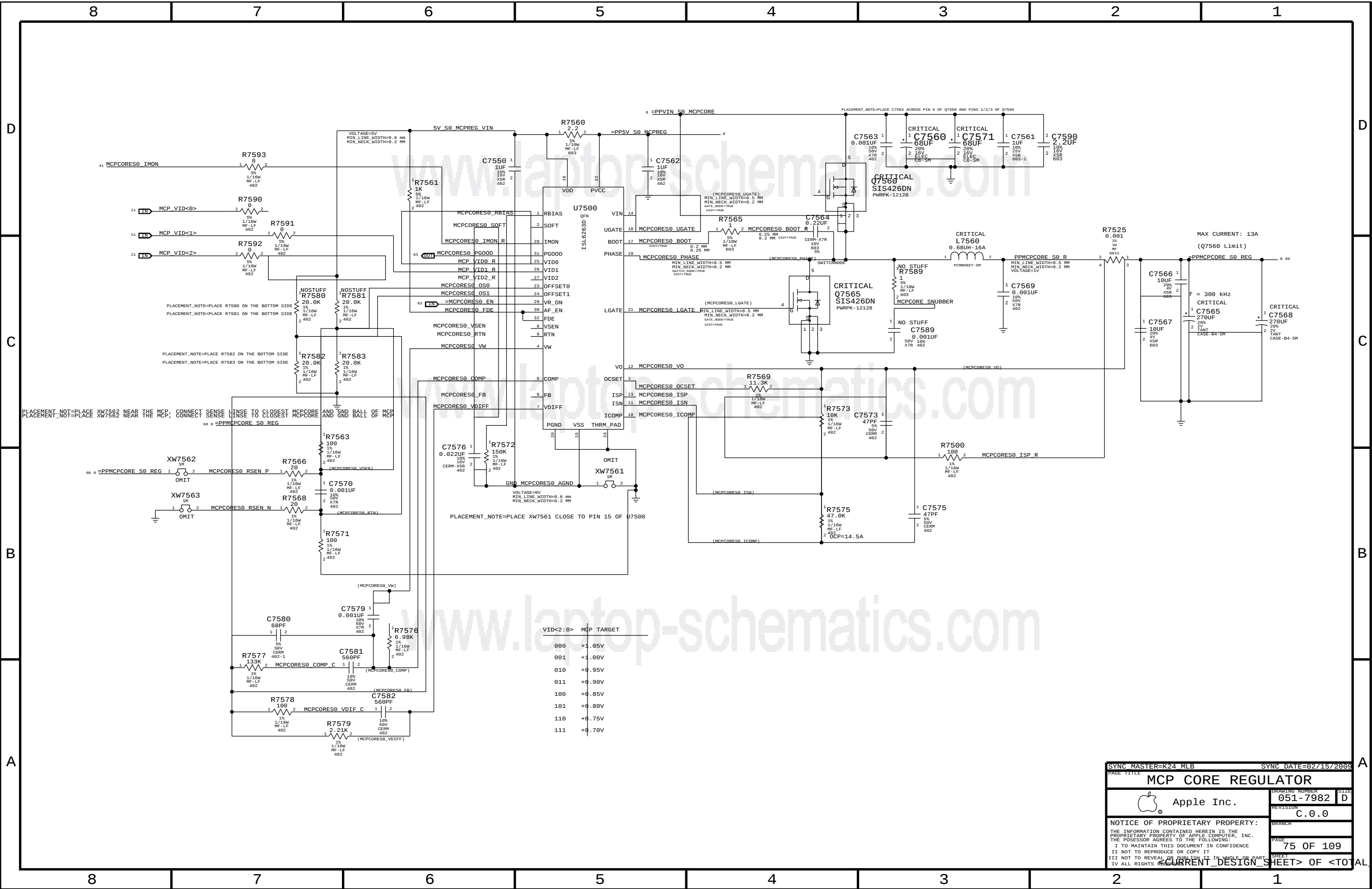
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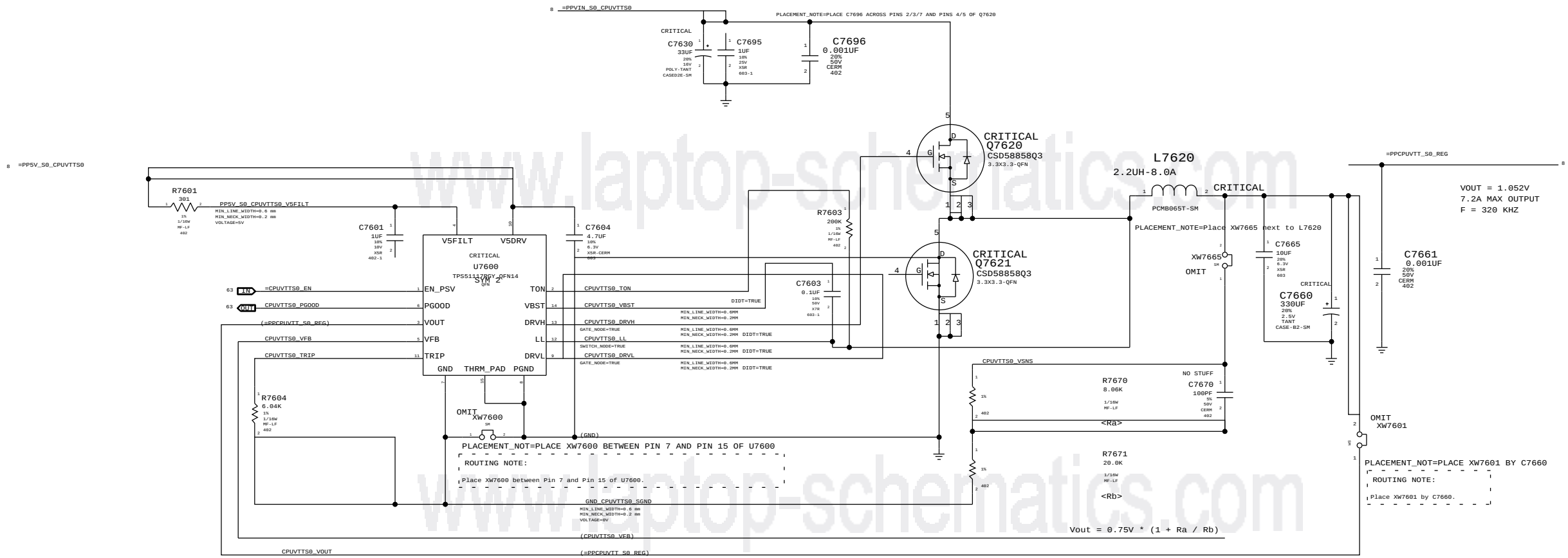
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CPUVTT POWER SUPPLY

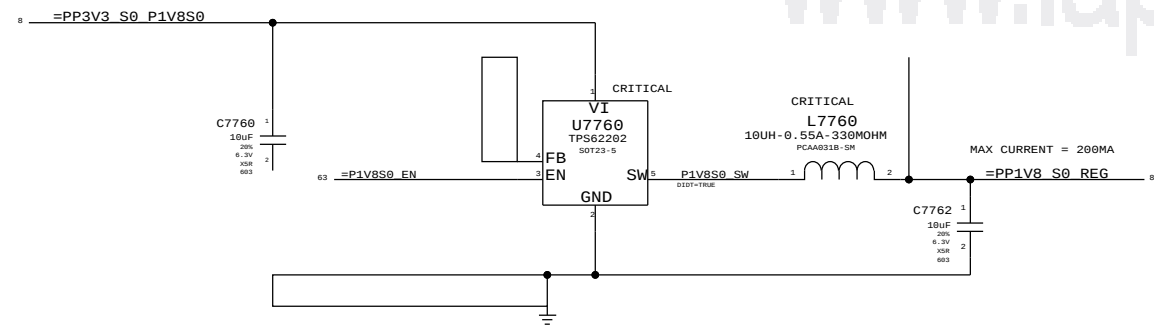
www.laptop-schematics.com



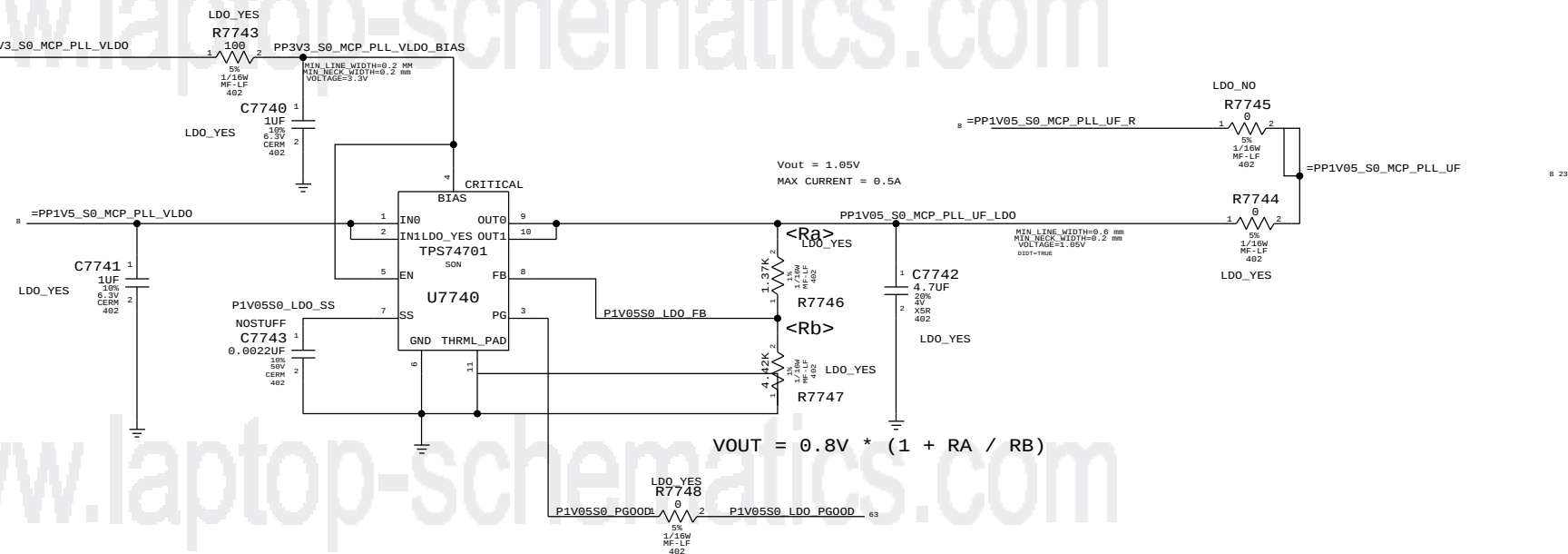
SYNC MASTER=K24 MLB		SYNC DATE=02/04/2009	
PAGE TITLE		CPU VTT(1.05V) SUPPLY	
DRAWING NUMBER		051-7982	D
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PAGE		76 OF 109	
SHEET			
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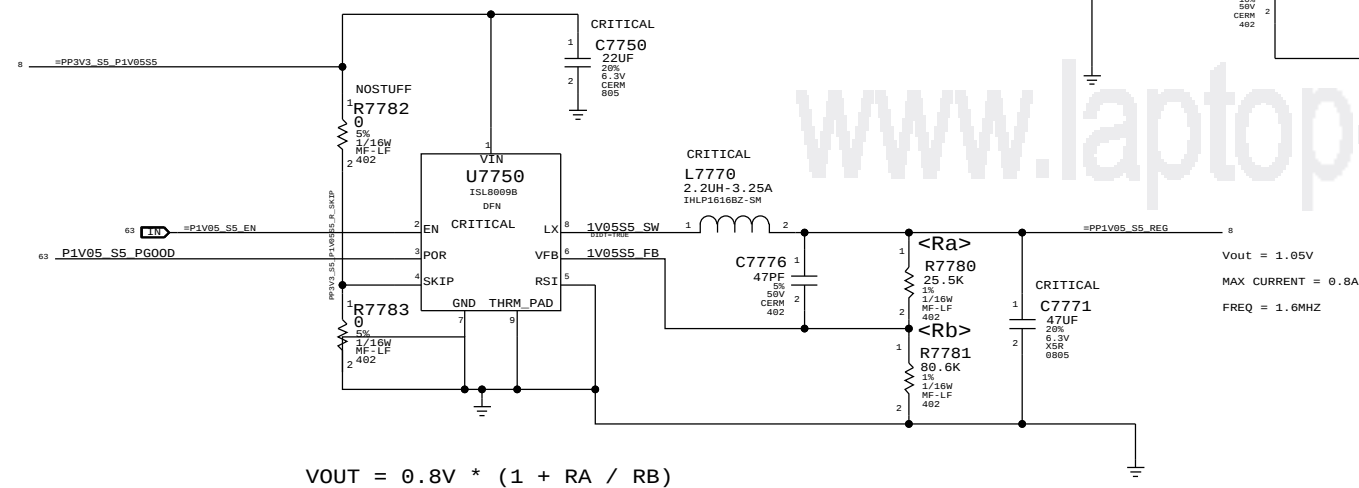
1.8V S0 SWITCHER



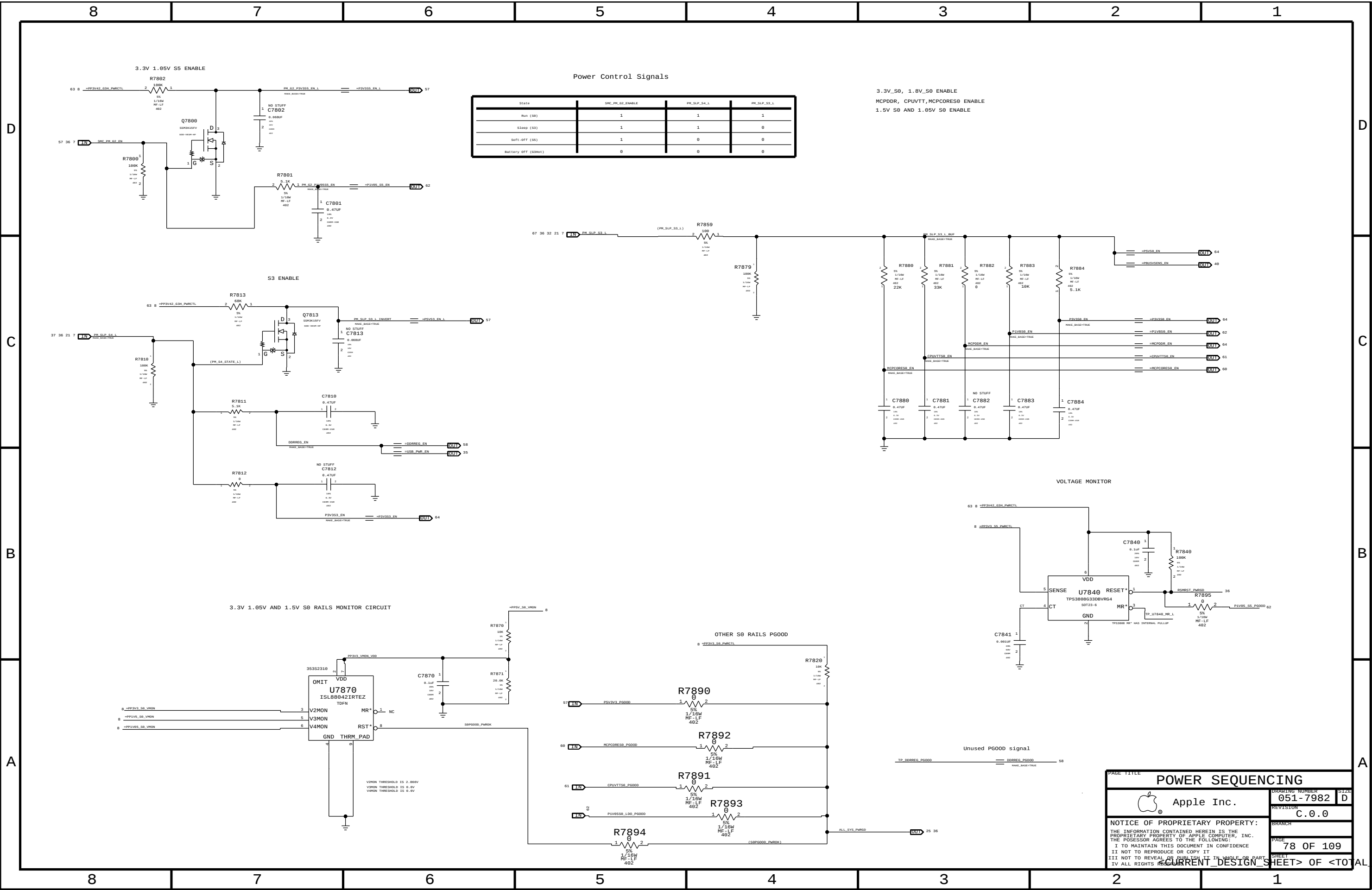
1.05V S0 PLL LDO

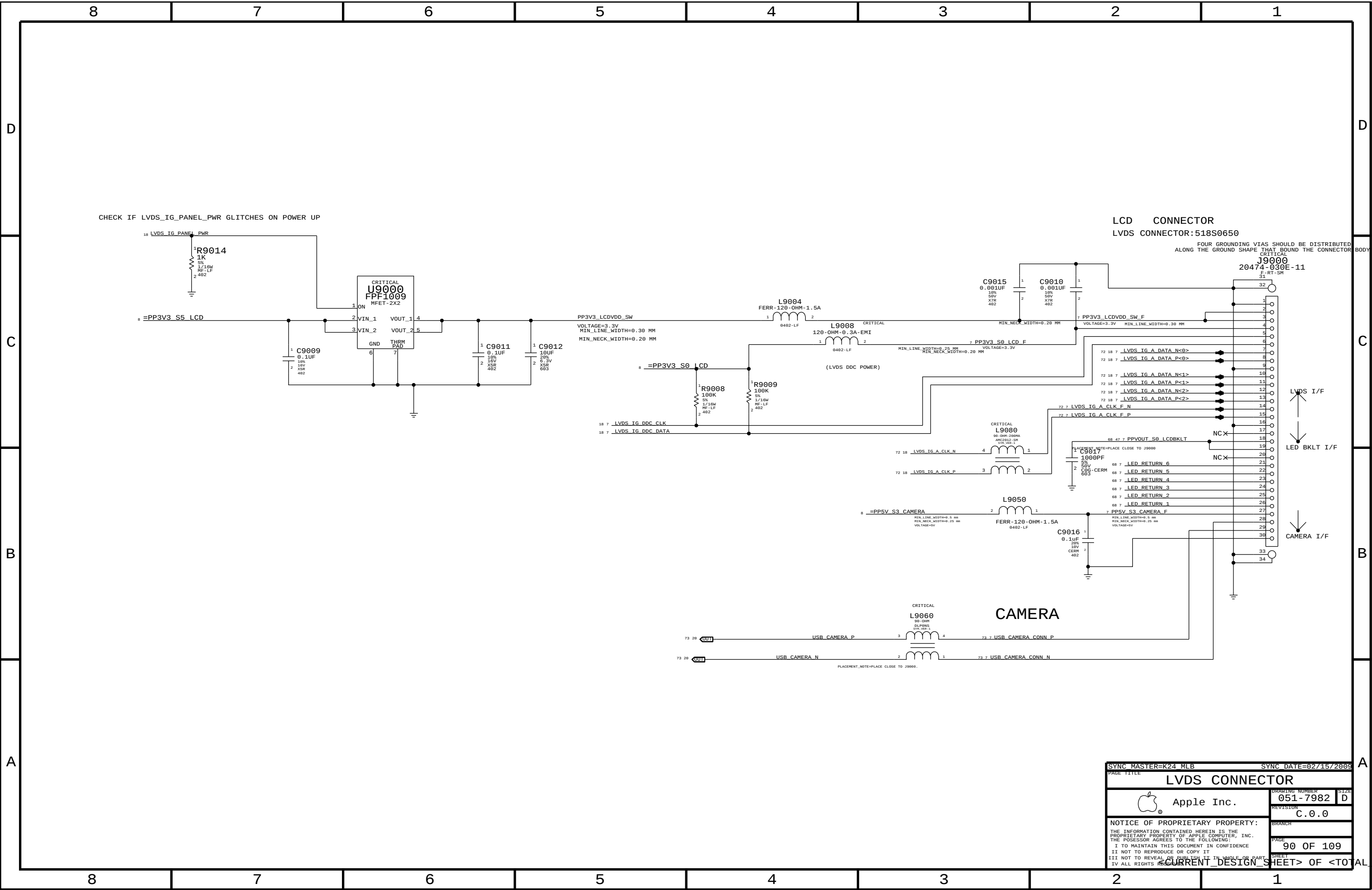


MCP 1.05V S5 (AUXC) SUPPLY



SYNC MASTER=K24 MLB		SYNC DATE=03/24/2009	
PAGE TITLE		DRAWING NUMBER	
MISC POWER SUPPLIES		051-7982	
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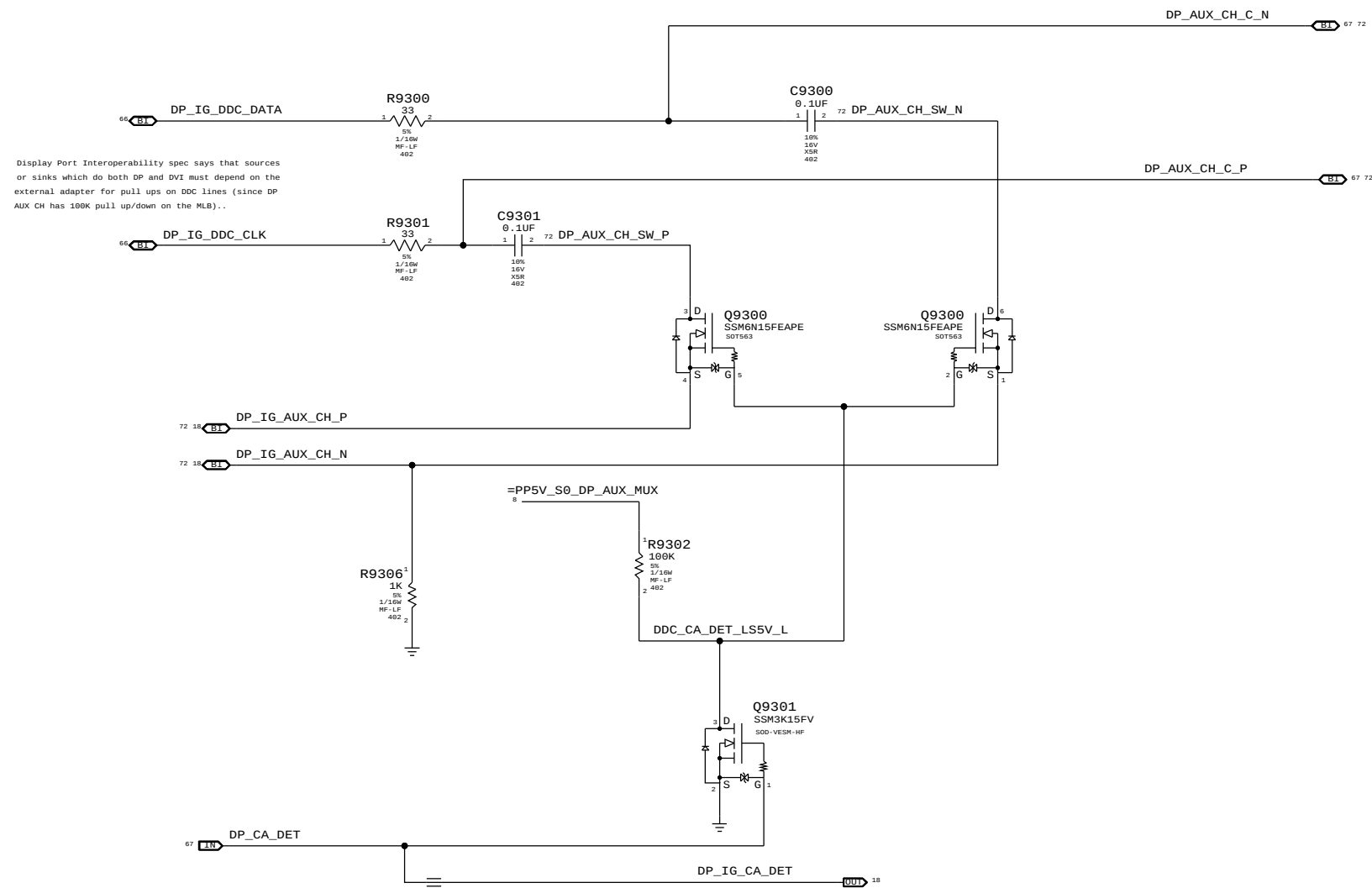




SYNC MASTER=K24 MLB		SYNC DATE=02/15/2009	
PAGE TITLE			
LVDS CONNECTOR			
	Apple Inc.	DRAWING NUMBER	051-7982
		SIZE	D
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66	==MCP_HDMI_TXD_P<22>	DP_ML_P<22>	67
67	==MCP_HDMI_TXD_N<22>	MAKE_BASE+TRUE	67
68	==MCP_HDMI_TXD_P<23>	DP_ML_P<23>	67
69	==MCP_HDMI_TXD_N<23>	MAKE_BASE+TRUE	67
70	==MCP_HDMI_TXD_P<24>	DP_ML_P<24>	67
71	==MCP_HDMI_TXD_N<24>	MAKE_BASE+TRUE	67
72	==MCP_HDMI_TXD_P<25>	DP_ML_P<25>	67
73	==MCP_HDMI_TXD_N<25>	MAKE_BASE+TRUE	67
74	==MCP_HDMI_TXD_P<26>	DP_ML_P<26>	67
75	==MCP_HDMI_TXD_N<26>	MAKE_BASE+TRUE	67
76	==MCP_HDMI_TXD_P<27>	DP_ML_P<27>	67
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78	==MCP_HDMI_TXD_P<28>	DP_ML_P<28>	67
79	==MCP_HDMI_TXD_N<28>	MAKE_BASE+TRUE	67
80	==MCP_HDMI_TXD_P<29>	DP_ML_P<29>	67
81	==MCP_HDMI_TXD_N<29>	MAKE_BASE+TRUE	67
82	==MCP_HDMI_TXD_P<30>	DP_ML_P<30>	67
83	==MCP_HDMI_TXD_N<30>	MAKE_BASE+TRUE	67
84	==MCP_HDMI_TXD_P<31>	DP_ML_P<31>	67
85	==MCP_HDMI_TXD_N<31>	MAKE_BASE+TRUE	67
86	==MCP_HDMI_TXD_P<32>	DP_ML_P<32>	67
87	==MCP_HDMI_TXD_N<32>	MAKE_BASE+TRUE	67
88	==MCP_HDMI_TXD_P<33>	DP_ML_P<33>	67
89	==MCP_HDMI_TXD_N<33>	MAKE_BASE+TRUE	67
90	==MCP_HDMI_TXD_P<34>	DP_ML_P<34>	67
91	==MCP_HDMI_TXD_N<34>	MAKE_BASE+TRUE	67
92	==MCP_HDMI_TXD_P<35>	DP_ML_P<35>	67
93	==MCP_HDMI_TXD_N<35>	MAKE_BASE+TRUE	67

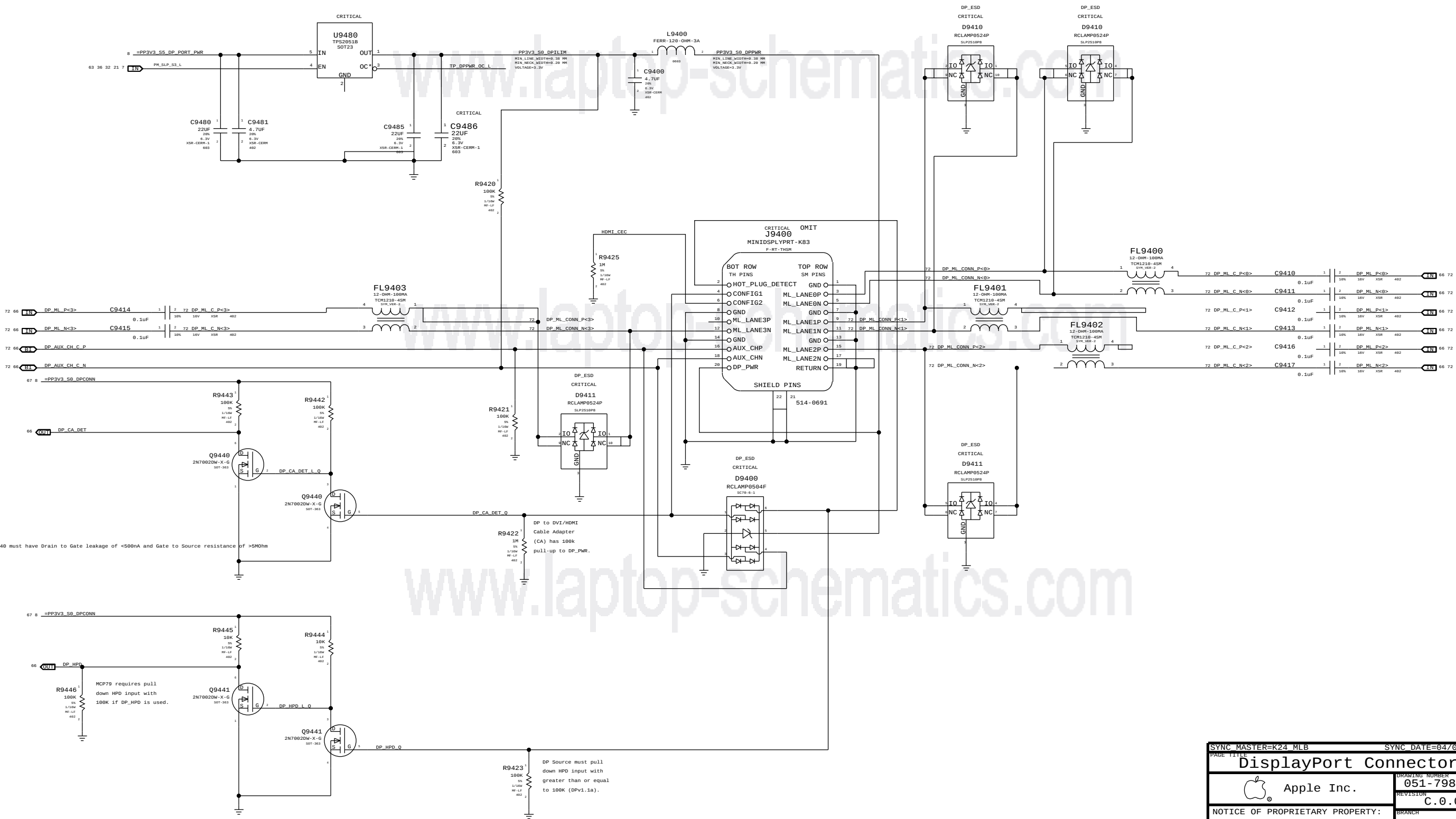


Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)..

SYNCH MASTER=K24 MLB		SYNCH DATE=04/06/2009	
PAGE TITLE			
DISPLAYPORT SUPPORT			
 Apple Inc.	DRAWING NUMBER	SIZE	
	051-7982	D	
	REVISION	C.0.0	
BRANCH			
PAGE			
93 OF 109			
SHEET			
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Port Power Switch

POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SUMBOLS
HAVE BEEN USED BEACUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES



SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE		DisplayPort Connector	
DRAWING NUMBER		051-7982	SIZE D
REVISION		C.0.0	BRANCH
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CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

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<table> <tr> <th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr> <tr> <td>MEM_A05</td><td>*</td><td>=A0_OHM_SE</td><td>=A0_OHM_SE</td><td>=A0_OHM_SE</td><td>=A0_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr> <tr> <td>MEM_A05_VDD</td><td>*</td><td>=A0_OHM_SE</td><td>=A0_OHM_SE</td><td>=A0_OHM_SE</td><td>=A0_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr> <tr> <td>MEM_700</td><td>*</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td></tr> <tr> <td>MEM_700_VDD</td><td>*</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td><td>=70_OHM_DIFF</td></tr> </table>				PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	MEM_A05	*	=A0_OHM_SE	=A0_OHM_SE	=A0_OHM_SE	=A0_OHM_SE	=STANDARD	=STANDARD	MEM_A05_VDD	*	=A0_OHM_SE	=A0_OHM_SE	=A0_OHM_SE	=A0_OHM_SE	=STANDARD	=STANDARD	MEM_700	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	MEM_700_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	<table> <tr> <th>NET_TYPE</th><th>PHYSICAL</th><th>SPACING</th><th></th></tr> <tr><td>MEM_A_CLK</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_CLK_P<5..0></td></tr> <tr><td>MEM_A_CLK</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_CLK_N<5..0></td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_CKE<3..0></td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_CS_L<3..0></td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_ODT<3..0></td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_A<14..0></td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_BA<2..0></td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_RAS_L</td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_CAS_L</td></tr> <tr><td>MEM_A_CMT1</td><td>MEM_A05_VDD</td><td>MEM_A05</td><td>MEM_A_WE_L</td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<7..0></td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<15..8></td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<23..16></td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<31..24></td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<39..32></td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<47..40></td></tr> <tr><td>MEM_A_DQ_BUFFER</td><td>MEM_A05</td><td>MEM_DATA</td><td>MEM_A_DQ<55..48></td></tr> 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<tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<1></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<1></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<2></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<2></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<3></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<3></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<4></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<4></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<5></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<5></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<6></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<6></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_P<7></td></tr> <tr><td>MEM_A_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_A_DQS_N<7></td></tr> <tr><td>MEM_B_CLK</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_CLK_P<5..0></td></tr> <tr><td>MEM_B_CLK</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_CLK_N<5..0></td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_CKE<3..0></td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_CS_L<3..0></td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_ODT<3..0></td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_A<14..0></td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_BA<2..0></td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_RAS_L</td></tr> <tr><td>MEM_B_CMT1</td><td>MEM_B05_VDD</td><td>MEM_B05</td><td>MEM_B_CAS_L</td></tr> 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<tr><td>MEM_B_DQS</td><td>MEM_700</td><td>MEM_DQS</td><td>MEM_B_DQS_N<2></td></tr> <tr><td>MEM_B_DQS</td><td></td></tr></table>	NET_TYPE	PHYSICAL	SPACING		MEM_A_CLK	MEM_A05_VDD	MEM_A05	MEM_A_CLK_P<5..0>	MEM_A_CLK	MEM_A05_VDD	MEM_A05	MEM_A_CLK_N<5..0>	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_CKE<3..0>	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_CS_L<3..0>	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_ODT<3..0>	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_A<14..0>	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_BA<2..0>	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_RAS_L	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_CAS_L	MEM_A_CMT1	MEM_A05_VDD	MEM_A05	MEM_A_WE_L	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<7..0>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<15..8>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<23..16>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<31..24>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<39..32>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<47..40>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<55..48>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DQ<63..56>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<0>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<1>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<2>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<3>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<4>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<5>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<6>	MEM_A_DQ_BUFFER	MEM_A05	MEM_DATA	MEM_A_DM<7>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<0>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<0>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<1>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<1>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<2>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<2>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<3>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<3>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<4>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<4>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<5>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<5>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<6>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<6>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_P<7>	MEM_A_DQS	MEM_700	MEM_DQS	MEM_A_DQS_N<7>	MEM_B_CLK	MEM_B05_VDD	MEM_B05	MEM_B_CLK_P<5..0>	MEM_B_CLK	MEM_B05_VDD	MEM_B05	MEM_B_CLK_N<5..0>	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_CKE<3..0>	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_CS_L<3..0>	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_ODT<3..0>	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_A<14..0>	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_BA<2..0>	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_RAS_L	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_CAS_L	MEM_B_CMT1	MEM_B05_VDD	MEM_B05	MEM_B_WE_L	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<7..0>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<15..8>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<23..16>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<31..24>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<39..32>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<47..40>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<55..48>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DQ<63..56>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<0>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<1>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<2>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<3>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<4>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<5>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<6>	MEM_B_DQ_BUFFER	MEM_B05	MEM_DATA	MEM_B_DM<7>	MEM_B_DQS	MEM_700	MEM_DQS	MEM_B_DQS_P<0>	MEM_B_DQS	MEM_700	MEM_DQS	MEM_B_DQS_N<0>	MEM_B_DQS	MEM_700	MEM_DQS	MEM_B_DQS_P<1>	MEM_B_DQS	MEM_700	MEM_DQS	MEM_B_DQS_N<1>	MEM_B_DQS	MEM_700	MEM_DQS	MEM_B_DQS_P<2>	MEM_B_DQS	MEM_700	MEM_DQS	MEM_B_DQS_N<2>	MEM_B_DQS	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																																																																																																																																																																																																			
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SYNCH MASTER=K24 MLB		SYNCH DATE=03/30/2009	
PAGE TITLE			
MCP Constraints 1			
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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_M1T_C0P	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_M1T_55S	*	=SS_OH1_SE	=SS_OH1_SE	=SS_OH1_SE	=SS_OH1_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	1	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18
	MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND 18
	MCP_CLK25M_BUF8	ENET_MII_SAS	MCP_BUF8_CLK	MCP_CLK25M_BUF8_R 18 32
		ENET_MII_SAS	MCP_BUF8_CLK	RTL8213_CLK25M_CKXTAL1 31 32
	ENET_TXP1_I	ENET_MII_SAS	ENET_MII2	ENET_INTR_I 18 32
	ENET_MDIO	ENET_MII_SAS	ENET_MII2	ENET_MDIO 18 32
	ENET_MDC	ENET_MII_SAS	ENET_MII2	ENET_MDC 18 32
	ENET_PWDOWN_I	ENET_MII_SAS	ENET_MII2	ENET_PWDOWN_I 18 32
		ENET_MII_SAS	ENET_MII2	ENET_CLK125M_RXCLK_R 31
	ENET_RXCLK	ENET_MII_SAS	ENET_MII2	ENET_CLK125M_RXCLK 18 32
		ENET_MII_SAS	ENET_MII2	ENET_RXD<3..0> 31
	ENET_RXD	ENET_MII_SAS	ENET_MII2	ENET_RXD<8> 18 32
	ENET_RXD_CTRM	ENET_MII_SAS	ENET_MII2	ENET_RXD<3..1> 18 32
	ENET_RXD	ENET_MII_SAS	ENET_MII2	ENET_RX_CTRM 18 32
		ENET_MII_SAS	ENET_MII2	ENET_RXCTL_R 31
		ENET_MII_SAS	ENET_MII2	ENET_CLK125M_TXCLK_R 31
	ENET_TXCLK	ENET_MII_SAS	ENET_MII2	ENET_CLK125M_TXCLK 18 32
	ENET_TXD0	ENET_MII_SAS	ENET_MII2	ENET_TXD<8> 18 32
	ENET_TXD	ENET_MII_SAS	ENET_MII2	ENET_TXD<3..1> 18 32
	ENET_TXD	ENET_MII_SAS	ENET_MII2	ENET_TX_CTRM 18 32
		ENET_MII_SAS	ENET_MII2	ENET_RESET_I 18 32
	ENET_MDI	ENET_MDI_1000	ENET_MDI	ENET_MDI_P<3..0> 31 32
		ENET_MDI_1000	ENET_MDI	ENET_MDI_N<3..0> 31 32
		ENET_MDI_1000	ENET_MDI	ENET_MDI_TRAN_P<3..0> 32
		ENET_MDI_1000	ENET_MDI	ENET_MDI_TRAN_N<3..0> 32

A

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	DIFFPAIR	CHGR_C50_R_P	56
	DIFFPAIR	CHGR_C50_R_N	56
	DIFFPAIR	CPUTHMSNS_D2_P	42
	DIFFPAIR	CPUTHMSNS_D2_N	42
	DIFFPAIR	CPU_THERMD_P	10 42
	DIFFPAIR	CPU_THERMD_N	10 42
	DIFFPAIR	TSNS_CPUVTT_P	41
	DIFFPAIR	TSNS_CPUVTT_N	
	DIFFPAIR	TSNS_HDD_P	34 47
	DIFFPAIR	TSNS_HDD_N	34 47
	DIFFPAIR	TSNS_HDD_R_P	47
	DIFFPAIR	TSNS_HDD_R_N	47
	DIFFPAIR	NCPTHMSNS_D2_P	42
	DIFFPAIR	NCPTHMSNS_D2_N	42
	DIFFPAIR	MCP_THMNODE_P	21 42
	DIFFPAIR	MCP_THMNODE_N	21 42
	DIFFPAIR	TSNS_ODD_P	34 47
	DIFFPAIR	TSNS_ODD_N	34 47
	DIFFPAIR	TSNS_ODD_R_P	47
	DIFFPAIR	TSNS_ODD_R_N	47
	DIFFPAIR	TSNS_AIRPORT_P	30 47
	DIFFPAIR	TSNS_AIRPORT_N	30 47
	DIFFPAIR	TSNS_AIRPORT_R_P	47
	DIFFPAIR	TSNS_AIRPORT_R_N	47
	DIFFPAIR	TSNS_IVS_S3_P	47 58
	DIFFPAIR	TSNS_IVS_S3_N	47 58
	DIFFPAIR	TSNS_IVS_S3_R_P	47
	DIFFPAIR	TSNS_IVS_S3_R_N	47
	DIFFPAIR	TSNS_LCDBKLT_P	47 68
	DIFFPAIR	TSNS_LCDBKLT_N	47 68

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K84 SPECIAL CONSTRAINTS			
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	K84 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS								
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION	
	TOP, 15L2, 15L3, 15L4, 15L5, 15L6, 15L7, 15L8, 15L9, 15L10, 15L11, BOTTOM				NO_TYPE, BGA_P1MM		MM	15.5.1	
D	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM	
	STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
	55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	58_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM				
	58_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	49_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.100 MM				
	49_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM				
	27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD	
C	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	70_OHM_DIFF	15L3, 15L4, 15L6, 15L10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	90_OHM_DIFF	15L3, 15L4, 15L6, 15L10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	100_OHM_DIFF	15L3, 15L4, 15L6, 15L10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	100_OHM_DIFF_HDD	15L3, 15L4, 15L6, 15L10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM	
B	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	110_OHM_DIFF	15L3, 15L4, 15L6, 15L10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	
A									
	8	7	6	5	4	3	2	1	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_FCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSB	FSB_DSB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_405	BGA_P1MM	STANDARD
MEM_405_VDD	BGA_P1MM	STANDARD

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K84 RULE DEFINITIONS



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